

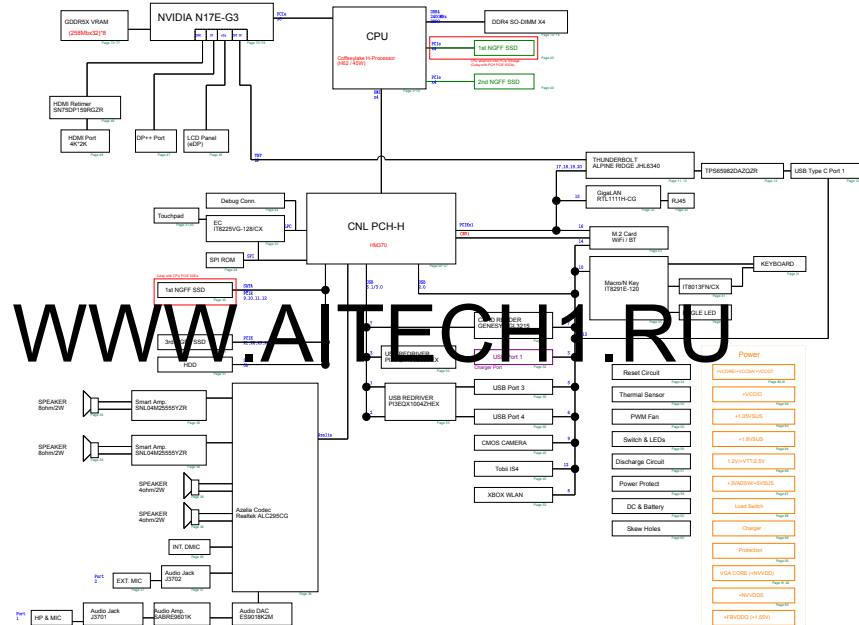
001_Bios Diagram
002_System Setting
003_CPU_DMI_PECI4CPD00
004_CPU_D0R4
005_CPU_GND
006_CPU_G0R5VD
007_
008_CPU_PWR(1)
009_CPU_PWR(2)
010_CPU_POWER_CAP
011_TST_Algine Ridge
012_TST_TPS6822Type C
013_TST_PWR
014_DMI_D0R4 SO-DIMM A(0)
015_DMI_D0R4 SO-DIMM B(0)
016_DMI_D0R4 SO-DIMM A(1)
017_DMI_D0R4 SO-DIMM B(1)
018_DMI_CAD0 Voltage
019_CPU_HSA_DMA032RTCTAG
020_PCH_PCIE SATA USB2 MISC
021_PCH_PCIE SATA USB2 MISC
022_PCH_CLK_LPC USB3
023_PCH_LVDS40DP
024_PCH_SPC_LNV
025_PCH_SPC
026_PCH_POWER_GND(1)
027_PCH_POWER_GND(2)
028_PCH_SPC_R0LCTH
029_TEST_POINT
030_MSC_IT2025
031_KBC_XB & TP
032_TST_Power Control
033_LAN_RTL811H-CG
034_LAN_R0R4_CON
035_Memory_R0CT_TT2021
036_AIO_ALC285
037_AIO_EXT Jack
038_AIO_INT_SPK
040_NGFF_SSD_PCIE_CON
041_NGFF_SSD_PCIE_CON_3
042_CR_GL3215
043_
044_BUG_LPC
045_HF_CON & Table_G4_CON
046_
047_Display Port
048_HDMI
049_
050_FAN_Thermal Sensor & Fan
051_HDD
052_USB3.0 Port
053_NGFF_NL4N & BT & XBCX
054_USB3.0 Port
055_LED & Switch
057_DSD_Discharge
058_Power Protect
059_SAR
060_DC & BAT IN
061_+Power Button_X0_BD
064_+LED_X0_BD
065_ME_V0B conn & NUT
066_
067_
068_
069_
070_GPU_PCIE IF
071_GPU_POWER
072_GPU_FRAME BUFFER
073_VRAM_CHANNEL A
074_VRAM_CHANNEL B
075_VRAM_CHANNEL C
076_VRAM_CHANNEL D
077_VRAM_CAP

080_PWK_COFFEEAKE (1)
081_PWK_COFFEEAKE (2)
082_PWK_VCCO
083_PWK_+1.05VUS
084_PWK_+1.05VUS
085_PWK_+1.2V-VTT2.5V
087_PWK_+3VACSW-V5VUS
088_PWK_LOAD SWITC
089_PWK_CHARGER
090_PWK_PROTECTION
091_PWK_MNVDD(1)
092_PWK_MNVDD(2)
093_PWK_MNVDD(3)
094_PWK_+0.5VDDQ
095_PWK_+0.5V_FAN
097_PWK_PEX_VDD
098_PWK_PFC

100_Power On T.ming-AC mode
101_Power On T.ming-DC mode

G703Gi Block Diagram

Coffeelaake H Platform



WWW.AITECH1.RU

Year	Month	Day	Event	Location	Time	Notes
1990	Jan	1
1990	Jan	2
1990	Jan	3
1990	Jan	4
1990	Jan	5
1990	Jan	6
1990	Jan	7
1990	Jan	8
1990	Jan	9
1990	Jan	10
1990	Jan	11
1990	Jan	12
1990	Jan	13
1990	Jan	14
1990	Jan	15
1990	Jan	16
1990	Jan	17
1990	Jan	18
1990	Jan	19
1990	Jan	20
1990	Jan	21
1990	Jan	22
1990	Jan	23
1990	Jan	24
1990	Jan	25
1990	Jan	26
1990	Jan	27
1990	Jan	28
1990	Jan	29
1990	Jan	30
1990	Jan	31
1990	Feb	1
1990	Feb	2
1990	Feb	3
1990	Feb	4
1990	Feb	5
1990	Feb	6
1990	Feb	7
1990	Feb	8
1990	Feb	9
1990	Feb	10
1990	Feb	11
1990	Feb	12
1990	Feb	13
1990	Feb	14
1990	Feb	15
1990	Feb	16
1990	Feb	17
1990	Feb	18
1990	Feb	19
1990	Feb	20
1990	Feb	21
1990	Feb	22
1990	Feb	23
1990	Feb	24
1990	Feb	25
1990	Feb	26
1990	Feb	27
1990	Feb	28
1990	Mar	1
1990	Mar	2
1990	Mar	3
1990	Mar	4
1990	Mar	5
1990	Mar	6
1990	Mar	7
1990	Mar	8
1990	Mar	9
1990	Mar	10
1990	Mar	11
1990	Mar	12
1990	Mar	13
1990	Mar	14
1990	Mar	15
1990	Mar	16
1990	Mar	17
1990	Mar	18
1990	Mar	19
1990	Mar	20
1990	Mar	21
1990	Mar	22
1990	Mar	23
1990	Mar	24
1990	Mar	25
1990	Mar	26
1990	Mar	27
1990	Mar					

Year	Country	Year of admission	Country of origin	Age group	Gender	Year
1999	USA	1999	USA	18-24	Male	1999
1999	USA	1999	USA	25-34	Male	1999
1999	USA	1999	USA	35-44	Male	1999
1999	USA	1999	USA	45-54	Male	1999
1999	USA	1999	USA	55-64	Male	1999
1999	USA	1999	USA	65-74	Male	1999
1999	USA	1999	USA	75+	Male	1999
1999	USA	1999	USA	18-24	Female	1999
1999	USA	1999	USA	25-34	Female	1999
1999	USA	1999	USA	35-44	Female	1999
1999	USA	1999	USA	45-54	Female	1999
1999	USA	1999	USA	55-64	Female	1999
1999	USA	1999	USA	65-74	Female	1999
1999	USA	1999	USA	75+	Female	1999
1999	USA	1999	USA	18-24	Both	1999
1999	USA	1999	USA	25-34	Both	1999
1999	USA	1999	USA	35-44	Both	1999
1999	USA	1999	USA	45-54	Both	1999
1999	USA	1999	USA	55-64	Both	1999
1999	USA	1999	USA	65-74	Both	1999
1999	USA	1999	USA	75+	Both	1999
1999	USA	1999	USA	18-24	Both	1999
1999	USA	1999	USA	25-34	Both	1999
1999	USA	1999	USA	35-44	Both	1999
1999	USA	1999	USA	45-54	Both	1999
1999	USA	1999	USA	55-64	Both	1999
1999	USA	1999	USA	65-74	Both	1999
1999	USA	1999	USA	75+	Both	1999
1999	USA	1999	USA	18-24	Both	1999
1999	USA	1999	USA	25-34	Both	1999
1999	USA	1999	USA	35-44	Both	1999
1999	USA	1999	USA	45-54	Both	1999
1999	USA	1999	USA	55-64	Both	1999
1999	USA	1999	USA	65-74	Both	1999
1999	USA	1999	USA	75+	Both	1999
1999	USA	1999	USA	18-24	Both	1999
1999	USA	1999	USA	25-34	Both	1999
1999	USA	1999	USA	35-44	Both	1999
1999	USA	1999	USA	45-54	Both	1999
1999	USA	1999	USA	55-64	Both	1999
1999	USA	1999	USA	65-74	Both	1999
1999	USA	1999	USA	75+	Both	1999
1999	USA	1999	USA	18-24	Both	1999
1999	USA	1999	USA	25-34	Both	1999
1999	USA	1999	USA	35-44	Both	1999
1999	USA	1999	USA	45-54	Both	1999
1999	USA	1999	USA	55-64	Both	1999
1999	USA	1999	USA	65-74	Both	1999
1999	USA	1999	USA	75+	Both	1999
1999	USA	1999	USA	18-24	Both	1999
1999	USA	1999	USA	25-34	Both	1999
1999	USA	1999	USA	35-44	Both	1999
1999	USA	1999	USA	45-54	Both	1999
1999	USA	1999	USA	55-64	Both	1999
1999	USA	1999	USA	65-74	Both	1999
1999	USA	1999	USA	75+	Both	1999
1999	USA	1999	USA	18-24	Both	1999
1999	USA	1999	USA	25-34	Both	1999
1999	USA	1999	USA	35-44	Both	1999
1999	USA	1999	USA	45-54	Both	1999
1999	USA	1999	USA	55-64	Both	1999
1999	USA	1999	USA	65-74	Both	1999
1999	USA	1999	USA	75+	Both	1999
1999	USA	1999	USA	18-24	Both	1999
1999	USA	1999	USA	25-34	Both	1999
1999	USA	1999	USA	35-44	Both	1999
1999	USA	1999	USA	45-54	Both	1999
1999	USA	1999	USA			

[illegible]

Year	Month	Day	Time	Location	Activity	Notes
2018	1	1	10:00	1000	1000	1000
2018	1	2	10:00	1000	1000	1000
2018	1	3	10:00	1000	1000	1000
2018	1	4	10:00	1000	1000	1000
2018	1	5	10:00	1000	1000	1000
2018	1	6	10:00	1000	1000	1000
2018	1	7	10:00	1000	1000	1000
2018	1	8	10:00	1000	1000	1000
2018	1	9	10:00	1000	1000	1000
2018	1	10	10:00	1000	1000	1000
2018	1	11	10:00	1000	1000	1000
2018	1	12	10:00	1000	1000	1000
2018	1	13	10:00	1000	1000	1000
2018	1	14	10:00	1000	1000	1000
2018	1	15	10:00	1000	1000	1000
2018	1	16	10:00	1000	1000	1000
2018	1	17	10:00	1000	1000	1000
2018	1	18	10:00	1000	1000	1000
2018	1	19	10:00	1000	1000	1000
2018	1	20	10:00	1000	1000	1000
2018	1	21	10:00	1000	1000	1000
2018	1	22	10:00	1000	1000	1000
2018	1	23	10:00	1000	1000	1000
2018	1	24	10:00	1000	1000	1000
2018	1	25	10:00	1000	1000	1000
2018	1	26	10:00	1000	1000	1000
2018	1	27	10:00	1000	1000	1000
2018	1	28	10:00	1000	1000	1000
2018	1	29	10:00	1000	1000	1000
2018	1	30	10:00	1000	1000	1000
2018	1	31	10:00	1000	1000	1000
2018	2	1	10:00	1000	1000	1000
2018	2	2	10:00	1000	1000	1000
2018	2	3	10:00	1000	1000	1000
2018	2	4	10:00	1000	1000	1000
2018	2	5	10:00	1000	1000	1000
2018	2	6	10:00	1000	1000	1000
2018	2	7	10:00	1000	1000	1000
2018	2	8	10:00	1000	1000	1000
2018	2	9	10:00	1000	1000	1000
2018	2	10	10:00	1000	1000	1000
2018	2	11	10:00	1000	1000	1000
2018	2	12	10:00	1000	1000	1000
2018	2	13	10:00	1000	1000	1000
2018	2	14	10:00	1000	1000	1000
2018	2	15	10:00	1000	1000	1000
2018	2	16	10:00	1000	1000	1000
2018	2	17	10:00	1000	1000	1000
2018	2	18	10:00	1000	1000	1000
2018	2	19	10:00	1000	1000	1000
2018	2	20	10:00	1000	1000	1000
2018	2	21	10:00	1000	1000	1000
2018	2	22	10:00	1000	1000	1000
2018	2	23	10:00	1000	1000	1000
2018	2	24	10:00	1000	1000	1000
2018	2	25				

Year	Month	Day	Event	Location	Time
2010	Jan	1	2010-01-01	2010-01-01	1:00
2010	Jan	2	2010-01-02	2010-01-02	1:00
2010	Jan	3	2010-01-03	2010-01-03	1:00
2010	Jan	4	2010-01-04	2010-01-04	1:00
2010	Jan	5	2010-01-05	2010-01-05	1:00
2010	Jan	6	2010-01-06	2010-01-06	1:00
2010	Jan	7	2010-01-07	2010-01-07	1:00
2010	Jan	8	2010-01-08	2010-01-08	1:00
2010	Jan	9	2010-01-09	2010-01-09	1:00
2010	Jan	10	2010-01-10	2010-01-10	1:00
2010	Jan	11	2010-01-11	2010-01-11	1:00
2010	Jan	12	2010-01-12	2010-01-12	1:00
2010	Jan	13	2010-01-13	2010-01-13	1:00
2010	Jan	14	2010-01-14	2010-01-14	1:00
2010	Jan	15	2010-01-15	2010-01-15	1:00
2010	Jan	16	2010-01-16	2010-01-16	1:00
2010	Jan	17	2010-01-17	2010-01-17	1:00
2010	Jan	18	2010-01-18	2010-01-18	1:00
2010	Jan	19	2010-01-19	2010-01-19	1:00
2010	Jan	20	2010-01-20	2010-01-20	1:00
2010	Jan	21	2010-01-21	2010-01-21	1:00
2010	Jan	22	2010-01-22	2010-01-22	1:00
2010	Jan	23	2010-01-23	2010-01-23	1:00
2010	Jan	24	2010-01-24	2010-01-24	1:00
2010	Jan	25	2010-01-25	2010-01-25	1:00
2010	Jan	26	2010-01-26	2010-01-26	1:00
2010	Jan	27	2010-01-27	2010-01-27	1:00
2010	Jan	28	2010-01-28	2010-01-28	1:00
2010	Jan	29	2010-01-29	2010-01-29	1:00
2010	Jan	30	2010-01-30	2010-01-30	1:00
2010	Jan	31	2010-01-31	2010-01-31	1:00

[illegible]

Year	Country	Age	Gender	Education	Occupation	Income	Health
2010	USA	25	Male	High School	Unemployed	\$10,000	Good
2010	USA	30	Female	College	Teacher	\$25,000	Good
2010	USA	35	Male	College	Engineer	\$40,000	Good
2010	USA	40	Female	College	Manager	\$50,000	Good
2010	USA	45	Male	College	Manager	\$60,000	Good
2010	USA	50	Female	College	Manager	\$70,000	Good
2010	USA	55	Male	College	Manager	\$80,000	Good
2010	USA	60	Female	College	Manager	\$90,000	Good
2010	USA	65	Male	College	Manager	\$100,000	Good
2010	USA	70	Female	College	Manager	\$110,000	Good
2010	USA	75	Male	College	Manager	\$120,000	Good
2010	USA	80	Female	College	Manager	\$130,000	Good
2010	USA	85	Male	College	Manager	\$140,000	Good
2010	USA	90	Female	College	Manager	\$150,000	Good
2010	USA	95	Male	College	Manager	\$160,000	Good
2010	USA	100	Female	College	Manager	\$170,000	Good

[illegible]

Year	Country	Population (millions)	Urban population (millions)	Urban population (%)	Population density (per sq km)	Population density (per sq mile)
1950	United States	150.7	80.0	53.1	26.3	68.0
1950	France	45.7	25.0	54.7	200.0	520.9
1950	Germany	68.7	35.0	50.9	234.0	603.8
1950	Japan	83.7	45.0	53.8	333.0	864.5
1950	India	361.0	100.0	27.7	147.0	381.0
1950	China	554.0	100.0	18.0	120.0	311.0
1950	United Kingdom	56.0	35.0	62.5	254.0	656.0
1950	Italy	45.7	25.0	54.7	200.0	520.9
1950	Canada	14.0	7.0	50.0	1.0	2.6
1950	Australia	10.0	5.0	50.0	0.3	0.8
1950	South Africa	4.0	2.0	50.0	0.1	0.3
1950	Argentina	16.0	8.0	50.0	1.0	2.6
1950	Brazil	70.0	35.0	50.0	1.0	2.6
1950	Mexico	20.0	10.0	50.0	1.0	2.6
1950	Colombia	10.0	5.0	50.0	1.0	2.6
1950	Venezuela	5.0	2.5	50.0	1.0	2.6
1950	Peru	10.0	5.0	50.0	1.0	2.6
1950	Ecuador	5.0	2.5	50.0	1.0	2.6
1950	Bolivia	5.0	2.5	50.0	1.0	2.6
1950	Paraguay	5.0	2.5	50.0	1.0	2.6
1950	Uruguay	3.0	1.5	50.0	1.0	2.6
1950	Chile	5.0	2.5	50.0	1.0	2.6
1950	Argentina	16.0	8.0	50.0	1.0	2.6
1950	Brazil	70.0	35.0	50.0	1.0	2.6
1950	Mexico	20.0	10.0	50.0	1.0	2.6
1950	Colombia	10.0	5.0	50.0	1.0	2.6
1950	Venezuela	5.0	2.5	50.0	1.0	2.6
1950	Peru	10.0	5.0	50.0	1.0	2.6
1950	Ecuador	5.0	2.5	50.0	1.0	2.6
1950	Bolivia	5.0	2.5	50.0	1.0	2.6
1950	Paraguay	5.0	2.5	50.0	1.0	2.6
1950	Uruguay	3.0	1.5	50.0	1.0	2.6
1950	Chile	5.0	2.5	50.0	1.0	2.6
1950	Argentina	16.0	8.0	50.0	1.0	2.6
1950	Brazil	70.0	35.0	50.0	1.0	2.6
1950	Mexico	20.0	10.0	50.0	1.0	2.6
1950	Colombia	10.0	5.0	50.0	1.0	2.6
1950	Venezuela	5.0	2.5	50.0	1.0	2.6
1950	Peru	10.0	5.0	50.0	1.0	2.6
1950	Ecuador	5.0	2.5	50.0	1.0	2.6
1950	Bolivia	5.0	2.5	50.0	1.0	2.6
1950	Paraguay	5.0	2.5	50.0	1.0	2.6
1950	Uruguay	3.0	1.5	50.0	1.0	2.6
1950	Chile	5.0	2.5	50.0	1.0	2.6
1950	Argentina	16.0	8.0	50.0	1.0	2.6
1950	Brazil	70.0	35.0	50.0	1.0	2.6
1950	Mexico	20.0	10.0	50.0	1.0	2.6
1950	Colombia	10.0	5.0	50.0	1.0	2.6
1950	Venezuela	5.0	2.5	50.0	1.0	2.6
1950	Peru	10.0	5.0	50.0	1.0	2.6
1950	Ecuador	5.0	2.5	50.0	1.0	2.6
1950	Bolivia	5.0	2.5	50.0	1.0	2.6
1950	Paraguay	5.0	2.5	50.0	1.0	2.6
1950	Uruguay	3.0	1.5	50.0	1.0	2.6
1950	Chile	5.0	2.5	50.0	1.0	2.6
1950	Argentina	16.0	8.0</			

Year	Month	Day	Time	Location	Activity	Notes
2018	1	1	10:00	Room 101	Classroom	First day of class
2018	1	2	10:00	Room 101	Classroom	Second day of class
2018	1	3	10:00	Room 101	Classroom	Third day of class
2018	1	4	10:00	Room 101	Classroom	Fourth day of class
2018	1	5	10:00	Room 101	Classroom	Fifth day of class
2018	1	6	10:00	Room 101	Classroom	Sixth day of class
2018	1	7	10:00	Room 101	Classroom	Seventh day of class
2018	1	8	10:00	Room 101	Classroom	Eighth day of class
2018	1	9	10:00	Room 101	Classroom	Ninth day of class
2018	1	10	10:00	Room 101	Classroom	Tenth day of class
2018	1	11	10:00	Room 101	Classroom	Eleventh day of class
2018	1	12	10:00	Room 101	Classroom	Twelfth day of class
2018	1	13	10:00	Room 101	Classroom	Thirteenth day of class
2018	1	14	10:00	Room 101	Classroom	Fourteenth day of class
2018	1	15	10:00	Room 101	Classroom	Fifteenth day of class
2018	1	16	10:00	Room 101	Classroom	Sixteenth day of class
2018	1	17	10:00	Room 101	Classroom	Seventeenth day of class
2018	1	18	10:00	Room 101	Classroom	Eighteenth day of class
2018	1	19	10:00	Room 101	Classroom	Nineteenth day of class
2018	1	20	10:00	Room 101	Classroom	Twentieth day of class
2018	1	21	10:00	Room 101	Classroom	Twenty-first day of class
2018	1	22	10:00	Room 101	Classroom	Twenty-second day of class
2018	1	23	10:00	Room 101	Classroom	Twenty-third day of class
2018	1	24	10:00	Room 101	Classroom	Twenty-fourth day of class
2018	1	25	10:00	Room 101	Classroom	Twenty-fifth day of class
2018	1	26	10:00	Room 101	Classroom	Twenty-sixth day of class
2018	1	27	10:00	Room 101	Classroom	Twenty-seventh day of class
2018	1	28	10:00	Room 101	Classroom	Twenty-eighth day of class
2018	1	29	10:00	Room 101	Classroom	Twenty-ninth day of class
2018	1	30	10:00	Room 101	Classroom	Thirtieth day of class
2018	2	1	10:00	Room 101	Classroom	First day of February
2018	2	2	10:00	Room 101	Classroom	Second day of February
2018	2	3	10:00	Room 101	Classroom	Third day of February
2018	2	4	10:00	Room 101	Classroom	Fourth day of February
2018	2	5	10:00	Room 101	Classroom	Fifth day of February
2018	2	6	10:00	Room 101	Classroom	Sixth day of February
2018	2	7	10:00	Room 101	Classroom	Seventh day of February
2018	2	8	10:00	Room 101	Classroom	Eighth day of February
2018	2	9	10:00	Room 101	Classroom	Ninth day of February
2018	2	10	10:00	Room 101	Classroom	Tenth day of February
2018	2	11	10:00	Room 101	Classroom	Eleventh day of February
2018	2	12	10:00	Room 101	Classroom	Twelfth day of February
2018	2	13	10:00	Room 101	Classroom	Thirteenth day of February
2018	2	14	10:00	Room 101	Classroom	Fourteenth day of February
2018	2	15	10:00	Room 101	Classroom	Fifteenth day of February
2018	2	16	10:00	Room 101	Classroom	Sixteenth day of February
2018	2	17	10:00	Room 101	Classroom	Seventeenth day of February
2018	2	18	10:00	Room 101	Classroom	Eighteenth day of February
2018	2	19	10:00	Room 101	Classroom	Nineteenth day of February
2018	2	20	10:00	Room 101	Classroom	Twentieth day of February
2018	2	21	10:00	Room 101	Classroom	Twenty-first day of February
2018	2	22	10:00	Room 101	Classroom	Twenty-second day of February
2018	2	23	10:00	Room 101	Classroom	Twenty-third day of February
2018	2	24	10:00	Room 101	Classroom	Twenty-fourth day of February
2018	2	25	10:00	Room 101	Classroom	Twenty-fifth day of February
2018	2	26				

Year	Department	Year	Department	Year	Department	Year	Department	Year	Department
2000	Department A	2001	Department B	2002	Department C	2003	Department D	2004	Department E
2005	Department F	2006	Department G	2007	Department H	2008	Department I	2009	Department J
2010	Department K	2011	Department L	2012	Department M	2013	Department N	2014	Department O
2015	Department P	2016	Department Q	2017	Department R	2018	Department S	2019	Department T
2020	Department U	2021	Department V	2022	Department W	2023	Department X	2024	Department Y
2025	Department Z	2026	Department A	2027	Department B	2028	Department C	2029	Department D
2030	Department E	2031	Department F	2032	Department G	2033	Department H	2034	Department I
2035	Department J	2036	Department K	2037	Department L	2038	Department M	2039	Department N
2040	Department O	2041	Department P	2042	Department Q	2043	Department R	2044	Department S
2045	Department T	2046	Department U	2047	Department V	2048	Department W	2049	Department X
2050	Department Y	2051	Department Z	2052	Department A	2053	Department B	2054	Department C
2055	Department D	2056	Department E	2057	Department F	2058	Department G	2059	Department H
2060	Department I	2061	Department J	2062	Department K	2063	Department L	2064	Department M
2065	Department N	2066	Department O	2067	Department P	2068	Department Q	2069	Department R
2070	Department S	2071	Department T	2072	Department U	2073	Department V	2074	Department W
2075	Department X	2076	Department Y	2077	Department Z	2078	Department A	2079	Department B
2080	Department C	2081	Department D	2082	Department E	2083	Department F	2084	Department G
2085	Department H	2086	Department I	2087	Department J	2088	Department K	2089	Department L
2090	Department M	2091	Department N	2092	Department O	2093	Department P	2094	Department Q
2095	Department R	2096	Department S	2097	Department T	2098	Department U	2099	Department V
2100	Department W	2101	Department X	2102	Department Y	2103	Department Z	2104	Department A

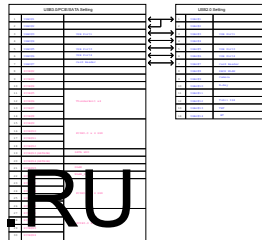
	Category	Item No.	Region Area	Percentage	Rate
Region	North	1	North	100%	100%
Region	South	2	South	100%	100%
Region	East	3	East	100%	100%
Region	West	4	West	100%	100%
Region	Central	5	Central	100%	100%
Region	North	6	North	100%	100%
Region	South	7	South	100%	100%
Region	East	8	East	100%	100%
Region	West	9	West	100%	100%
Region	Central	10	Central	100%	100%

[illegible]

2010	2009	2008	2007	2006	2005	2004	2003	2002	2001	2000	1999	1998	1997	1996	1995	1994	1993	1992	1991	1990	1989	1988	1987	1986	1985	1984	1983	1982	1981	1980	1979	1978	1977	1976	1975	1974	1973	1972	1971	1970	1969	1968	1967	1966	1965	1964	1963	1962	1961	1960	1959	1958	1957	1956	1955	1954	1953	1952	1951	1950	1949	1948	1947	1946	1945	1944	1943	1942	1941	1940	1939	1938	1937	1936	1935	1934	1933	1932	1931	1930	1929	1928	1927	1926	1925	1924	1923	1922	1921	1920	1919	1918	1917	1916	1915	1914	1913	1912	1911	1910	1909	1908	1907	1906	1905	1904	1903	1902	1901	1900	1899	1898	1897	1896	1895	1894	1893	1892	1891	1890	1889	1888	1887	1886	1885	1884	1883	1882	1881	1880	1879	1878	1877	1876	1875	1874	1873	1872	1871	1870	1869	1868	1867	1866	1865	1864	1863	1862	1861	1860	1859	1858	1857	1856	1855	1854	1853	1852	1851	1850	1849	1848	1847	1846	1845	1844	1843	1842	1841	1840	1839	1838	1837	1836	1835	1834	1833	1832	1831	1830	1829	1828	1827	1826	1825	1824	1823	1822	1821	1820	1819	1818	1817	1816	1815	1814	1813	1812	1811	1810	1809	1808	1807	1806	1805	1804	1803	1802	1801	1800	1799	1798	1797	1796	1795	1794	1793	1792	1791	1790	1789	1788	1787	1786	1785	1784	1783	1782	1781	1780	1779	1778	1777	1776	1775	1774	1773	1772	1771	1770	1769	1768	1767	1766	1765	1764	1763	1762	1761	1760	1759	1758	1757	1756	1755	1754	1753	1752	1751	1750	1749	1748	1747	1746	1745	1744	1743	1742	1741	1740	1739	1738	1737	1736	1735	1734	1733	1732	1731	1730	1729	1728	1727	1726	1725	1724	1723	1722	1721	1720	1719	1718	1717	1716	1715	1714	1713	1712	1711	1710	1709	1708	1707	1706	1705	1704	1703	1702	1701	1700	1699	1698	1697	1696	1695	1694	1693	1692	1691	1690	1689	1688	1687	1686	1685	1684	1683	1682	1681	1680	1679	1678	1677	1676	1675	1674	1673	1672	1671	1670	1669	1668	1667	1666	1665	1664	1663	1662	1661	1660	1659	1658	1657	1656	1655	1654	1653	1652	1651	1650	1649	1648	1647	1646	1645	1644	1643	1642	1641	1640	1639	1638	1637	1636	1635	1634	1633	1632	1631	1630	1629	1628	1627	1626	1625	1624	1623	1622	1621	1620	1619	1618	1617	1616	1615	1614	1613	1612	1611	1610	1609	1608	1607	1606	1605	1604	1603	1602</
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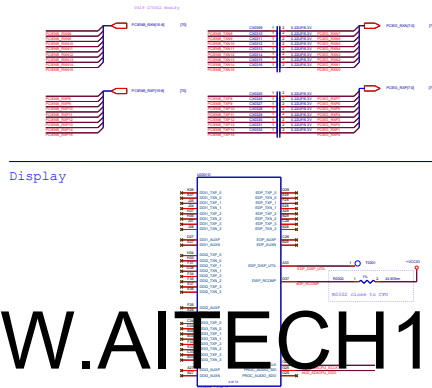
[illegible][illegible][illegible]

Device Identification		
Device Name		
SN	Device ID	Device Type
SN		
Device Information		
SN	Device ID	Device Type
SN		



871282_C62_P08_8_826_Vol. 1 Rev. 0_7, page 16

Figure 1. Schematic representation of the experimental design. The first part of the experiment consisted of a 10-min habituation period, followed by a 10-min baseline period, and then a 10-min test period. The test period was divided into two parts: a 5-min habituation period and a 5-min test period. The second part of the experiment consisted of a 10-min habituation period, followed by a 10-min baseline period, and then a 10-min test period. The test period was divided into two parts: a 5-min habituation period and a 5-min test period.



WWW.AITECH1.RU

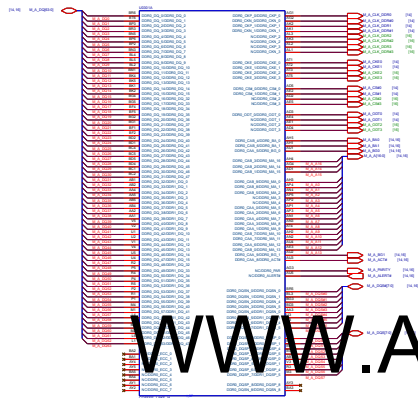
[illegible]

When HDA_CODEC[1:0], OISPA_CODEC interface is not implemented on the platform the signal pin(s) may be left unconnected.

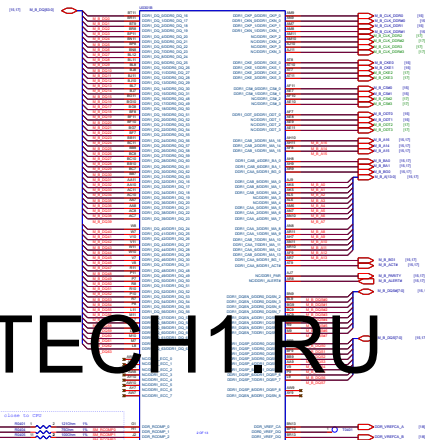
When HDA_CODEC[1:0], OSPA_CODEC interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLA and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. $\approx 2k\Omega$). PROC_AUDIO_SDO can be left unconnected.

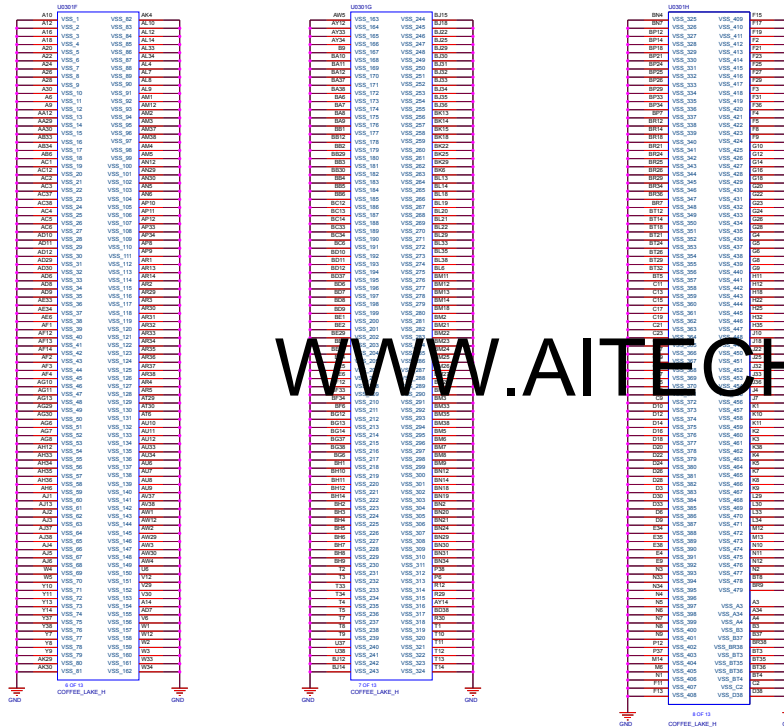
```
Memory Channel A
```

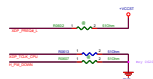
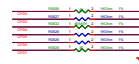
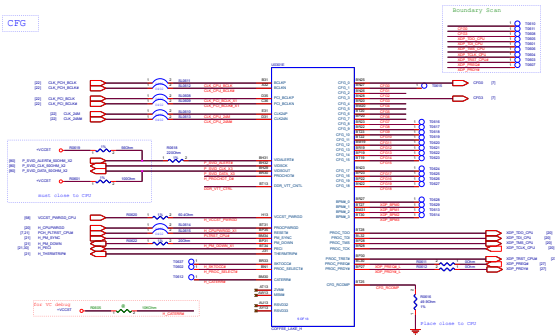


Memory Channel B



Main Board





CFG[0] : Stall reset sequence after PCU PLL lock until de-assert	Two
- 1 : (Default) Normal Operation; No stall	
- 0 : Stall	

CFG[1]: Reserved Configuration Lane
Reserved Configuration Lane
CFG[2]: PCI Express® Static x16 Lane Numbering Revision

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[5]: Reserved configuration lanes

Source: www.fpga.com

CFG[6]: eDP Enable

-1 : Disabled
-0 : Enabled

CFG[6.5]: PCI Express® Bifurcation
-00: 1 x8, 2 x4 PCI Express

- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7]: PEG Training

- 1: Default PEG Train Immediately Following RESET# de-assertion
- 0: PEG Wait for lock for training

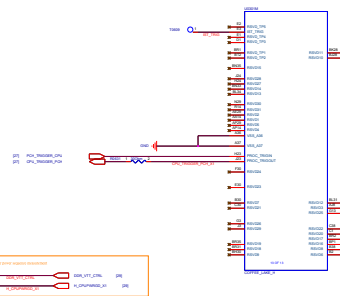
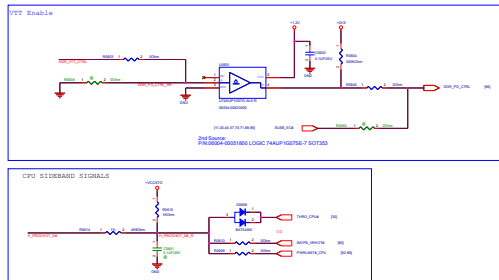
CFG(19:8) : Reserved Configuration Lines

Removed Configuration Lines

Refer : Intel SR043, CPU_Volt_Regs, Table 6-7, 9.1

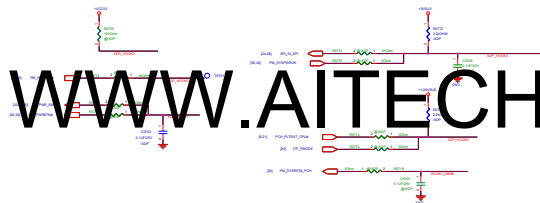
WWW.AITECH1.RU

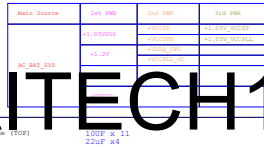
System Memory Power Gate Control:
Disables the platform memory VTT regulator in C8 and deeper and S3.





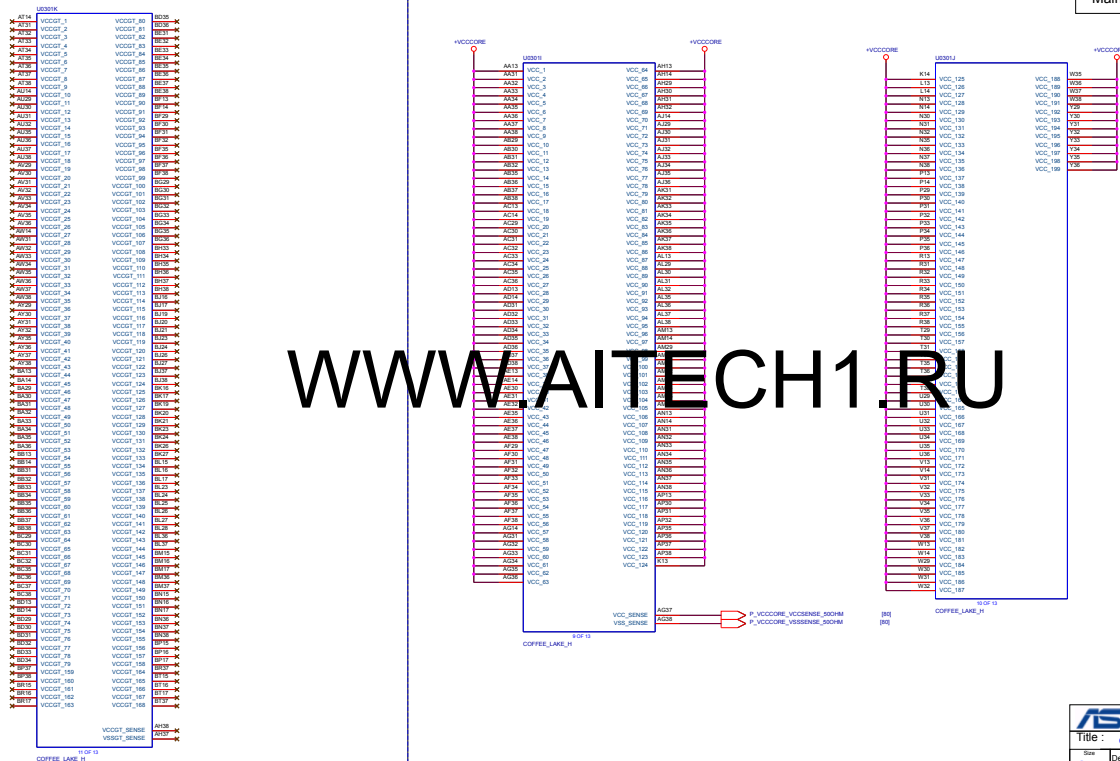
WWW.AITECH1.RU



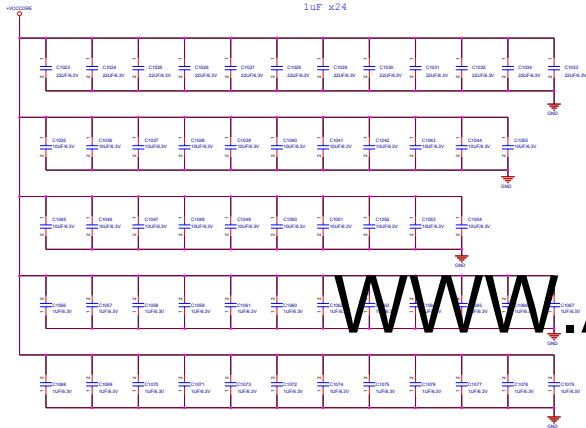


WWW.AITECH1.RU



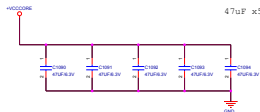


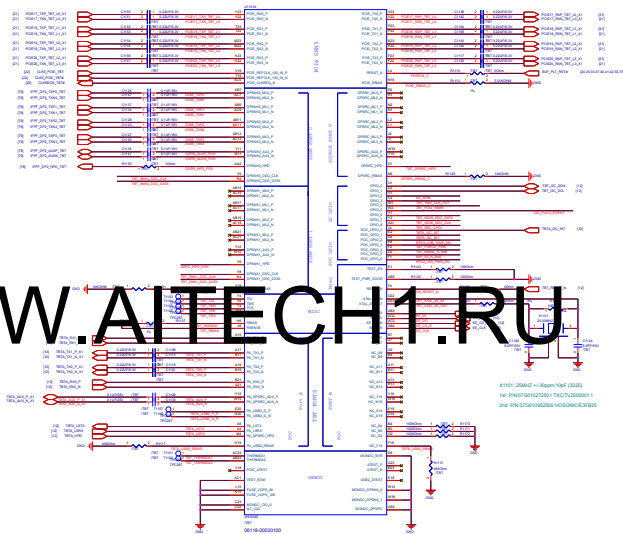
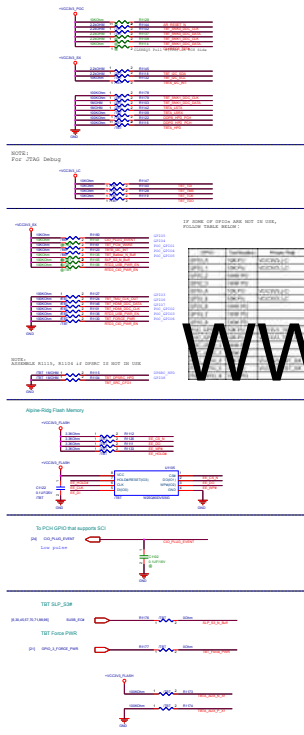
+VCCCORE DECAPS Place Back Side (TOP)

22uF x12
10uF x21
1uF x24

+VCCCORE cap near CPU

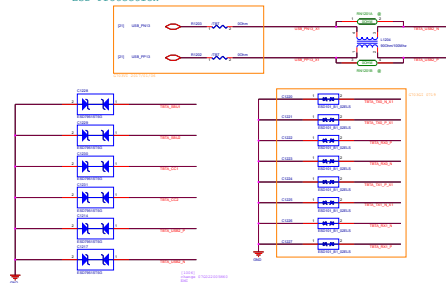
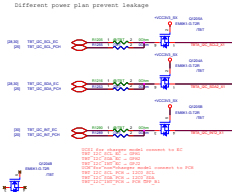
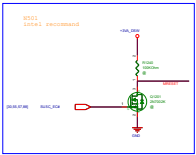
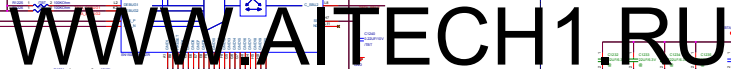
47uF x5

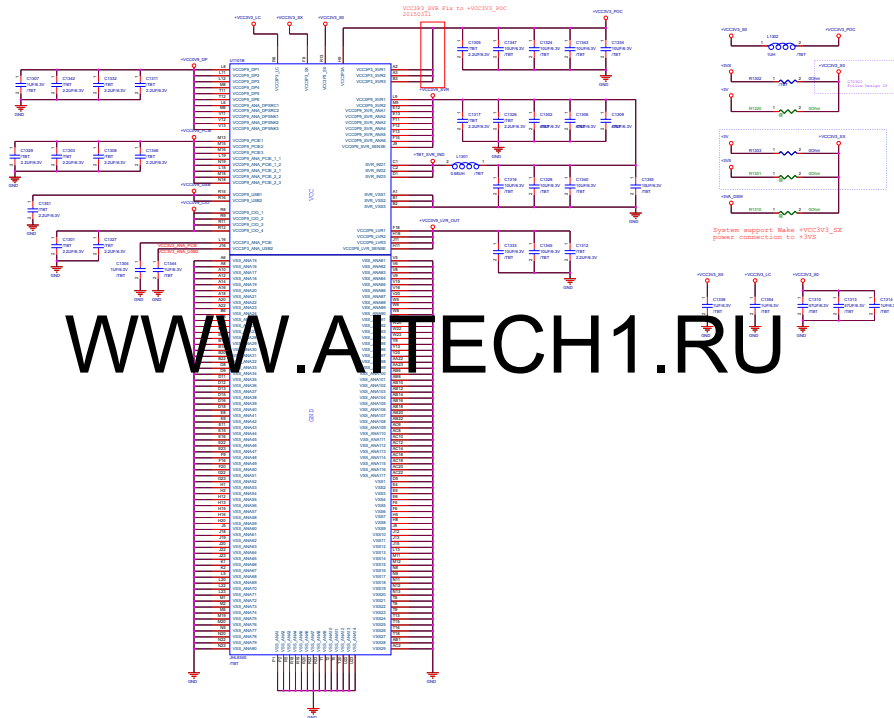




File	Translation
MUNDO.000	CARD
MUNDO.000000.0	CARD
MUNDO.000000.1	CARD
MUNDO.000000.2	CARD
MUNDO.000.0	CARD
MUNDO.000.1	CARD
TEST.000	CARD
FLIST.VOIR.00	CARD
FLIST.VOIR.000	CARD
ATTEST.000	01.04.1980
ATTEST.000	01.04.1980
PCIE.ATTEST	01.04.1980

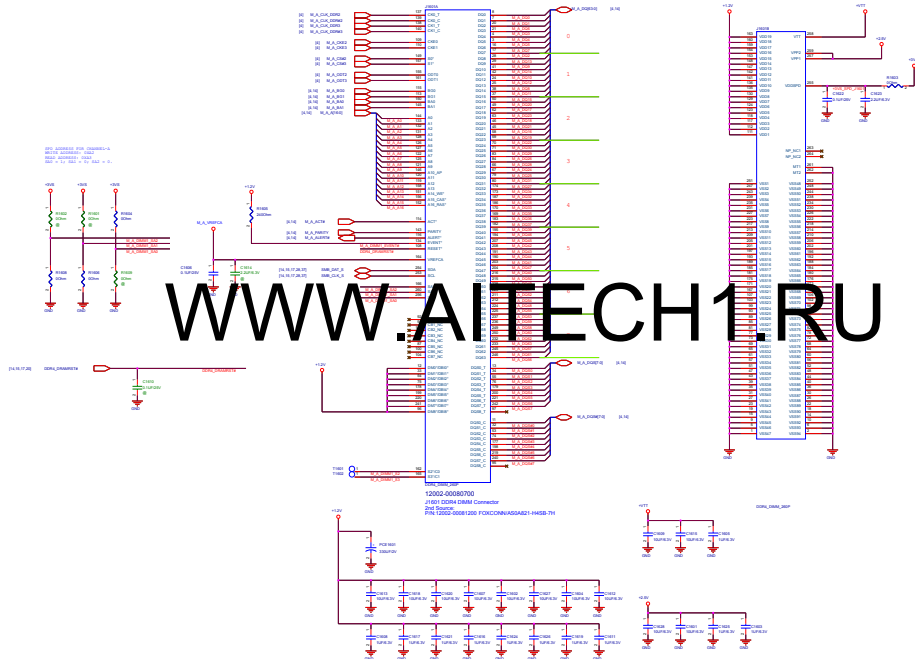




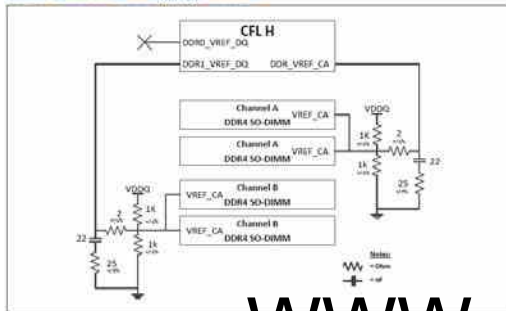


SODIMM CHA-DIMM1
TOP H4.0mm STD (J1601)

Main Board

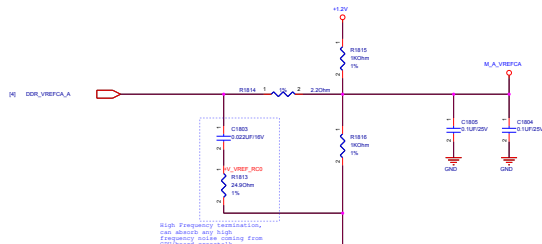


CFL'H DDR4 SO-DIMM V_{REF-CA} Overview



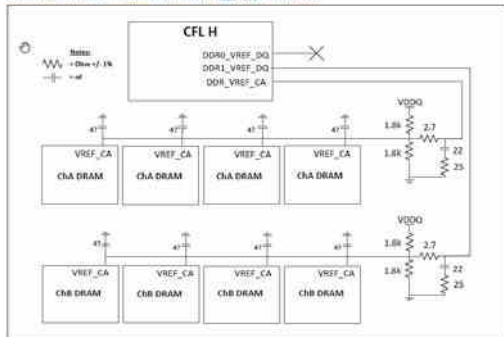
Vref for CBA_D1000
CBA_D1001

Main Board

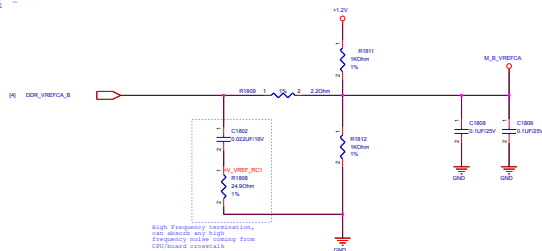


WWW.AITECH1.RU

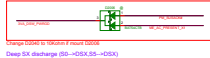
CFL H DDR4 x16 Memory Down V_{REF-CA} Overview



Vref for CBA_D1000
CBA_D1001



ASUS		Project Name	Rev
G703GI			R2.1
Title : CFL-H_DIM_CADesign_R1.3B			
Size	Dept.	ASUS&N COMPUTER INC. Engineer:	NB1 RD2 EE1
Date: Thursday, January 16, 2016	Sheet	16	of 103



G703GI Port Assignment

USB Setting

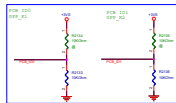
USB 2.0		USB 3.0	
USB2_00		USB3_01	USB3.0 type-A
USB2_02		USB3_02	USB3.0 type-A
USB2_04		USB3_03	USB3.0 type-A
USB2_05		USB3_04	USB3.0 type-A
USB2_06		USB3_05	USB3.0 type-A
USB2_07	Card Reader	USB3_07	Card Reader
USB2_08	Webcam	USB3_08	
USB2_09	Camera		
USB2_10	Hi-Key + HS-EC control		
USB2_11			
USB2_12	Test (H)		
USB2_13	Test		
USB2_14	BT		

PCIe/SATA Function define

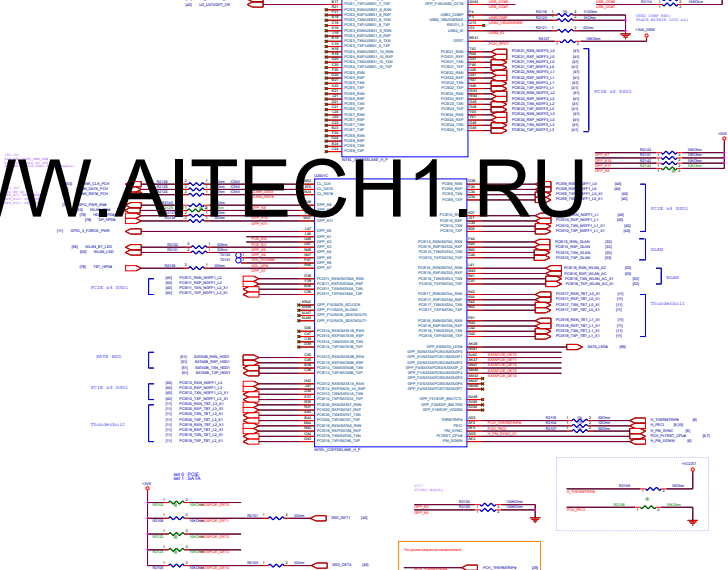
PCIe ID	Function	PCIe ID	Function
PCIe-01 (USB307)	USB Card Reader	PCIe-13 (SATA00)	SATA HDD
PCIe-02 (USB304)		PCIe-14 (SATA10)	SATA HDD
PCIe-03 (USB309)		PCIe-15 (SATA20)	SSAN
PCIe-04 (USB3010)		PCIe-16 (SATA30)	WLAN-AC
PCIe-05		PCIe-17 (SATA40)	
PCIe-06		PCIe-18 (SATA50)	Test (H)
PCIe-07		PCIe-19 (SATA60)	
PCIe-08		PCIe-20 (SATA70)	
PCIe-09		PCIe-21	
PCIe-10		PCIe-22	
PCIe-11 (SATA04)	PCIe SSD (H)	PCIe-23	PCIe SSD (H)
PCIe-12 (SATA14)	SATA SSD	PCIe-24	

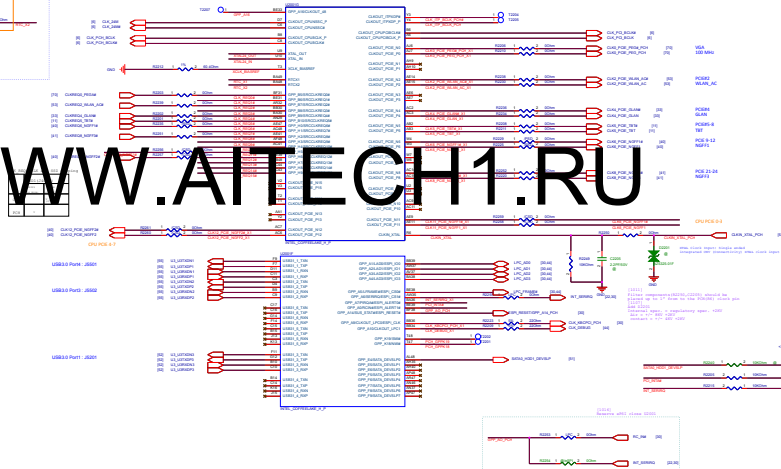
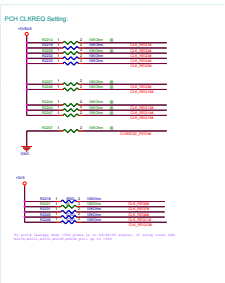
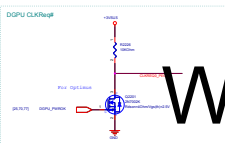
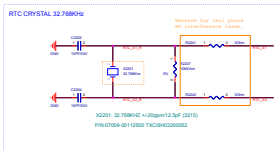
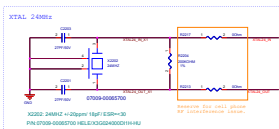
CLREQ ID	Function
CLREQ-0	DGPU
CLREQ-1	
CLREQ-2	WLAN-AC
CLREQ-3	
CLREQ-4	SSAN
CLREQ-5	Test
CLREQ-6	PCIe SSD(PCH)
CLREQ-7	
CLREQ-8	PCIe SSD(PCH)
CLREQ-9	
CLREQ-11	PCIe SSD(PCH)
CLREQ-12	PCIe SSD(PCH)
CLREQ-10/13/14/15	

Design IP



USB 3.0 Port for G703GI







G703GI display output from dGPU only,
so these strap are WC.
(Refer to PDG ch5.6, how to disable DDI)
If there is a MS-hybrid project, please notice the below strap

Strap => Display Port B Detected

PCB_GFP I6: weak internal pull down
0 : Port B is not detected. (Default)
1 : Port B is detected.

Strap => Display Port C Detected

PCB_GFP I8: weak internal pull down
0 : Port C is not detected. (Default)
1 : Port C is detected.

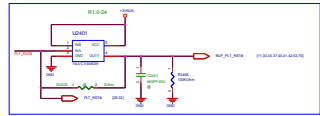
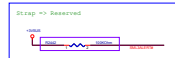
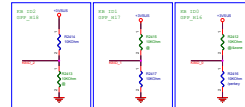
Strap => Display Port D Detected

PCB_GFP I10: weak internal pull down
0 : Port D is not detected. (Default)
1 : Port D is detected.

Strap => Display Port F Detected

PCB_GFP F23: weak internal pull down
0 : Port F is not detected. (Default)
1 : Port F is detected.

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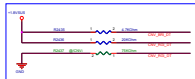


PCR_GPP_W12: weak internal pull down

Strap => eSPI Flash Sharing Mode

[illegible]

5. 將讀 BIOS ID 的 KB ID 讀取的部份, 額外加入 Reverse code, 以符合表 1 的 table



```

GPI 24(MOV REG 00):
This signal has a weak internal pull down.
0 = 10.4MHz STM frequency selected. (default)
1 = 140MHz STM frequency selected.

```

```

CPU: i486 CPU AGI 010
in Windows 95, scaling or pull-down is required.
0 = Integrated CPUID enable.
1 = Integrated CPUID disable.
[Local RAG]
AGI 02 has an automatic default CPUID mechanism,
please do not use external PG.
The CPU has an internal string IE 92 already.
Do not leave this bit blank,
if CPUID is not used, it still need a DSE like PG.

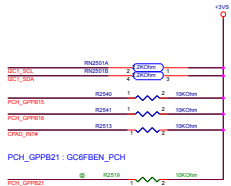
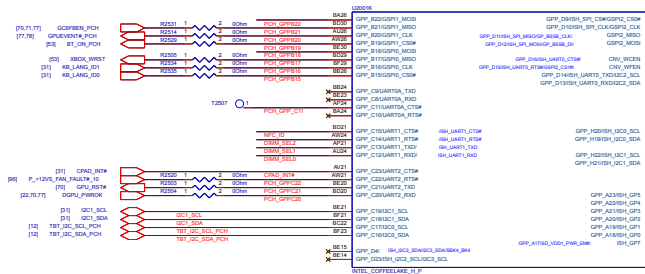
```

Q99 24:
The signal has a weak internal pull-down
0 = VCC/2 is converted to 0.0V rail

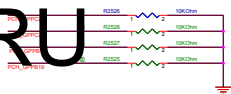
Strap => Reserved



Main Board



```
PCH_GPPC21 : GPU_RST#
PCH_GPPC20 : DGPU_PWROK
```



PCH_GPPB20 : GPU_EVENT#_PCH



```
Onboard Memory PCB-ID:
GPP_C12 => DIMM_SEL0
GPP_C13 => DIMM_SEL1
GPP_C14 => DIMM_SEL2
```

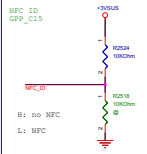


	Hynix (2Gb)	XXX (2Gb)	Micron (2Gb)
DIMM_SEL0			
DIMM_SEL1			
DIMM_SEL2			

	US	UK	JP
KB_LANG_ID0 (KB pin33)	1	0	0
KB_LANG_ID1 (KB pin34)	0	0	1

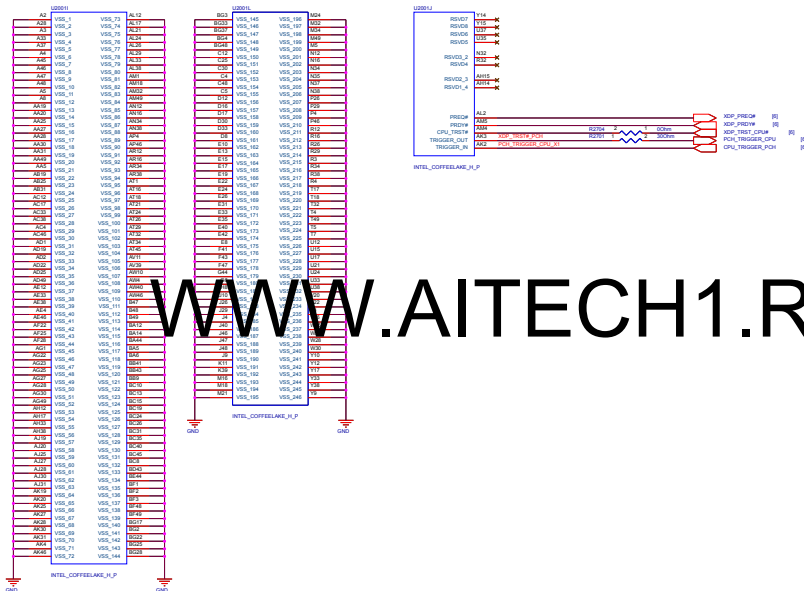
LA-PH 22-NC, PH-24-NC
LA-PH 22-JA-NC
LA-PH 22-ND, PH-24-NC

NFC ID
GPP C15

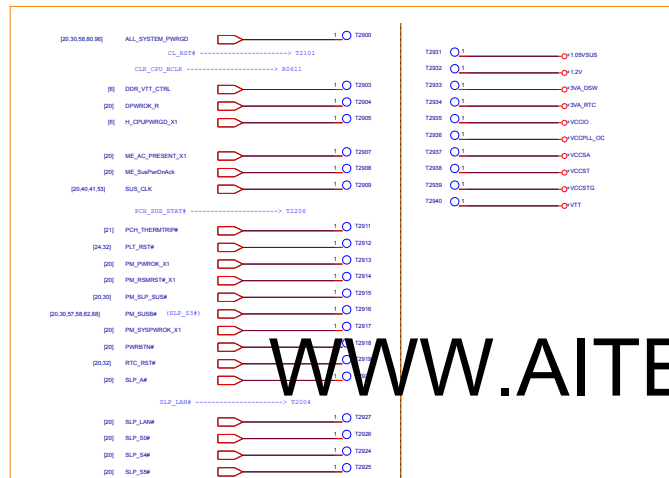


H:

L:



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+1.0V_VDDPLL -----> R0809
H_VCCST_PWRGD -----> R0820

T2931 1 1.0V_VDDPLL
T2932 1 1.2V
T2933 1 SWA_DSW
T2934 1 SWA_RTC
T2935 1 VCCD
T2936 1 VCCPLL_OC
T2937 1 VCCSA
T2938 1 VCCST
T2939 1 VCCSTG
T2940 1 VTT

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EC 8225

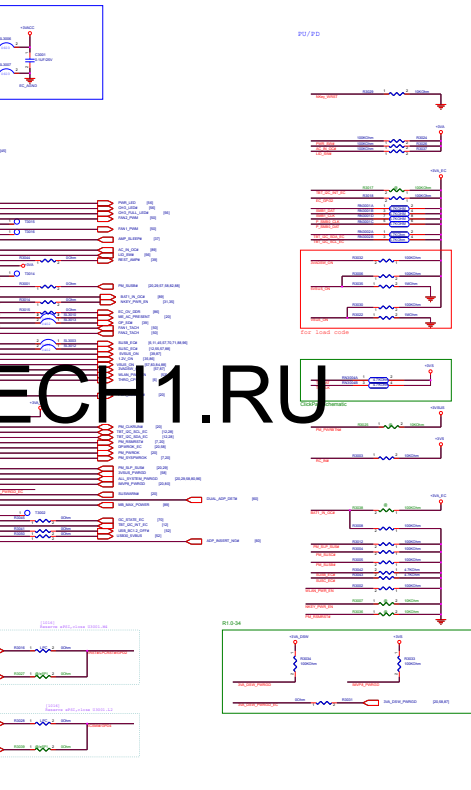
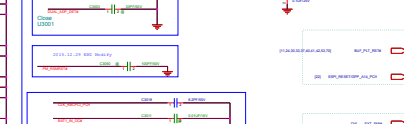
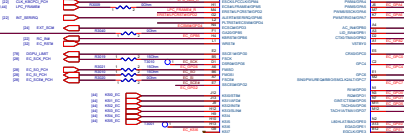
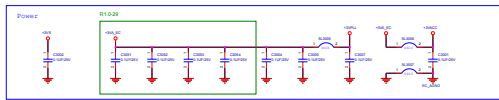
Only 3V Torrence

GP0[0,1,2,3,4,5,6]
GP0[3,4,5,6,7]
GP0[0,4,6,7]
GP0[4]
GP0[6,7]
GP0[0,17]
GP0[0,17]

Can be adjusted to
Open-Drain for post:

GP00-GP03
GP00-GP07
GP00-GP07
GP00-GP07
GP00-GP07
GP00-GP07
GP00-GP07
GP00-GP07

EC Region

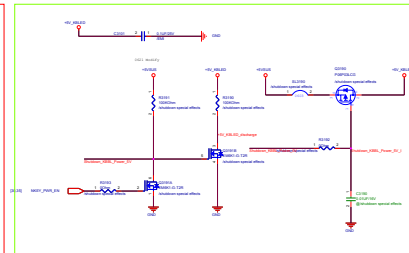
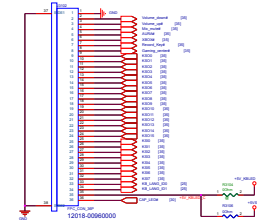


17th Version	ASUS 0/0
17th Version	ASUS 0/0

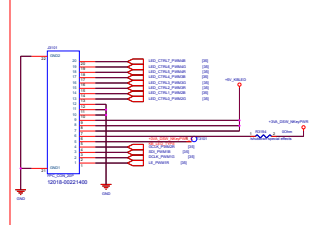
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Keyboard Connector



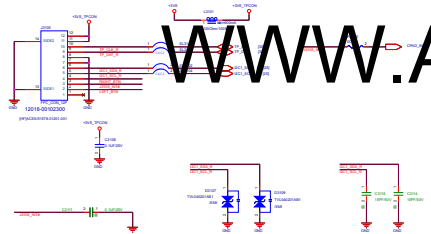
Keyboard LED Connector



To Touchpad

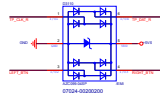
J3103 Touchpad Connector

1st Source: P/N 12018-0102300 ACE/S/0178-01201-001
 2nd Source: P/N 12018-0102100 ENTER Y16706-Y124-00L
 3rd Source: P/N 12018-0102260 ST ARCONN108E12-00000-A2-R
 4th Source: P/N 12018-0102400 P-TW0106475-1241-3

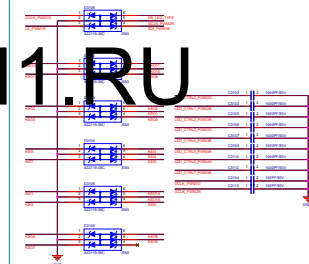


E30110 ESD Diode

1st Source: P/N 07024-0020000 AMAZING/ATC389-045P -BETG
 2nd Source: P/N 07024-00710000 NXP/PUS524V3



For EMI



To Touchpad Left,Right Button

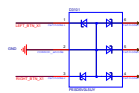


J3103 FPC 4Pin Conn.

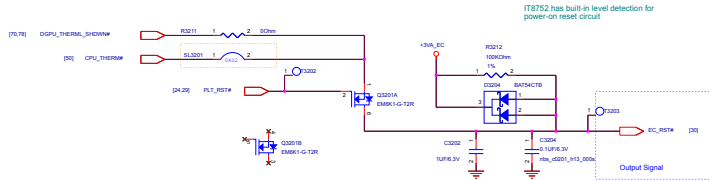
1st Source: P/N 12018-0000000 ENTER Y16156-Y04N-00L
 2nd Source: P/N 12018-0000100 ST ARCONN108E04-01000-A2-R

D4003 ESD Diode

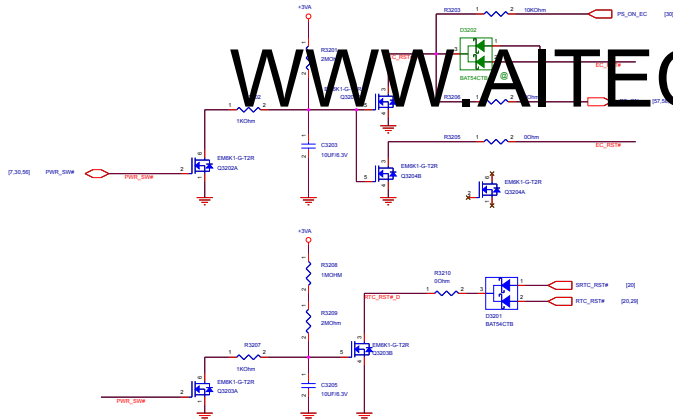
1st Source: P/N 07028162010 NXP SOT363
 2nd Source: P/N 07028162010 AMAZING SOT363-0L



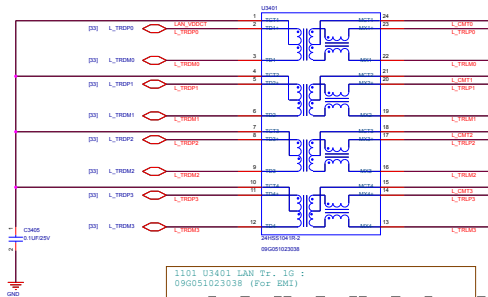
Thermal Policy



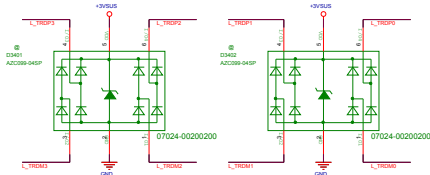
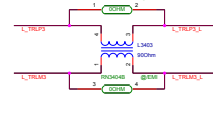
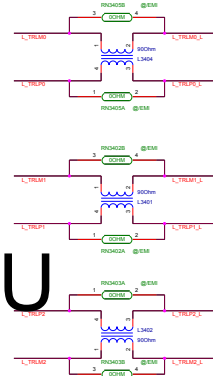
battery embedded (press pwr_sw 10sec, then reset ec)



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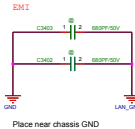
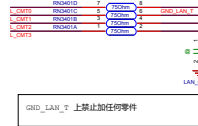
LAN Connector

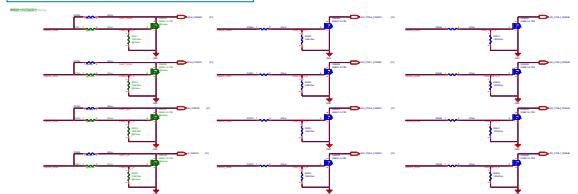
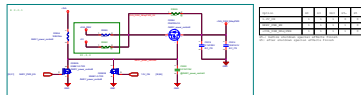


D3401,D3402 ESD Diode

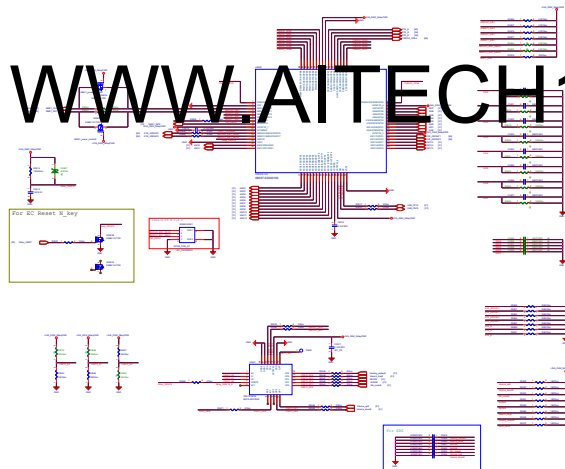
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP .R7G

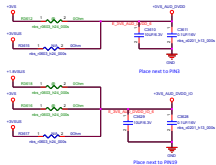
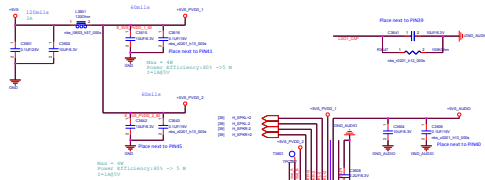
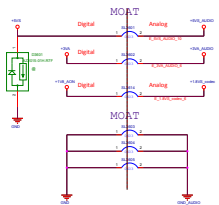
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



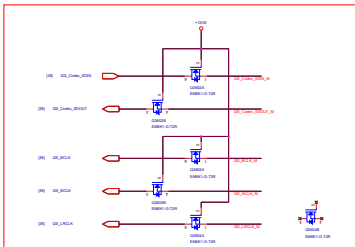
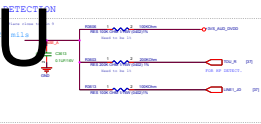
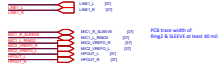
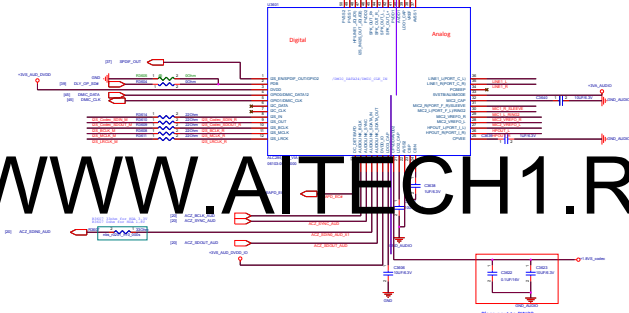


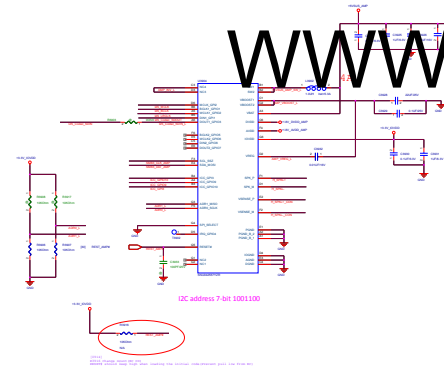
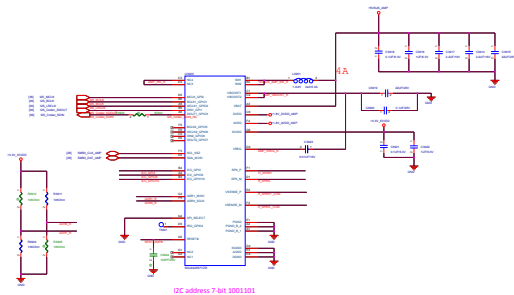
WWW.AITECH1.RU



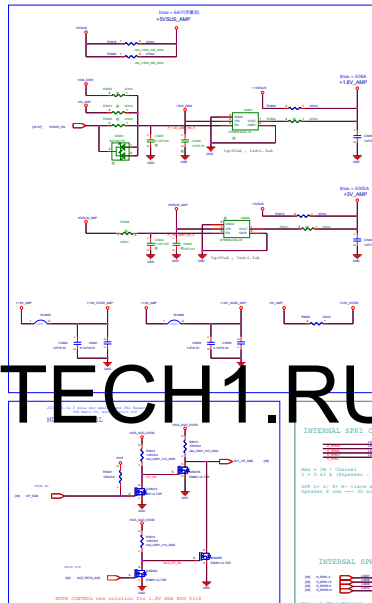


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11.4 Power Supply Sequencing

When the system is powered up, the power supply must be sequenced properly. The power supply must be sequenced properly to ensure that the system is powered up correctly. The power supply must be sequenced properly to ensure that the system is powered up correctly.



Figure 11.4 Power Supply Sequencing for Frequency and Bandwidth

When the system is powered up, the power supply must be sequenced properly. The power supply must be sequenced properly to ensure that the system is powered up correctly. The power supply must be sequenced properly to ensure that the system is powered up correctly.

11.5 Power Supplies

The A88M-LE requires three power supplies:

- Backup Input (terminal: VDD1)
 - Voltage: 2.0 V to 4.0 V
 - Max Current: 0.6 A to 0.8 A (typical)
- Backup Supply (terminal: VDD1)
 - Voltage: 1.0 V to 1.45 V
 - Max Current: 30 mA
- Digital Supply (terminal: VDD1)
 - Voltage: 1.0 V to 1.45 V
 - Max Current: 100 mA
- Digital I/O Supply (terminal: VDD1)
 - Voltage: 1.0 V to 1.45 V
 - Max Current: 30 mA

INTERNAL SPK1 Conn.

Max = 1W / Channel

T = 0.42 A (Speaker = 4 Ohm)

SPK on L+ R+ Pin: Speaker 4 Ohm

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

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Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

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Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

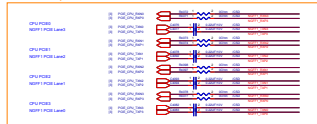
Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

Speaker 4 Ohm → 20 mV

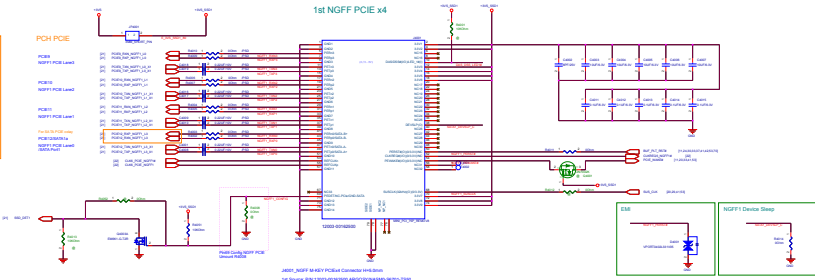
CPU PCIe Colay



PCIE POIE



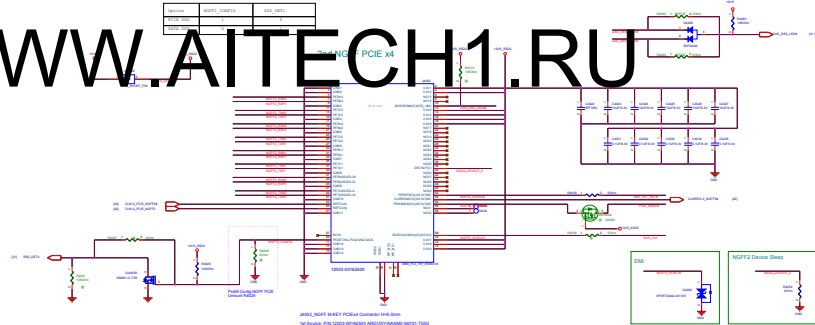
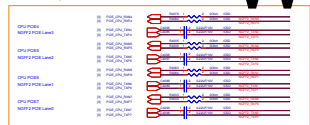
1st NGFF PCIe x4



ASUS NGFF M-KEY PCIe4 Connector HW-BOM
1st Source: P/N: 12000-02100000 AR9301/NA9300-96701-1580

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CPU PCIe Colay



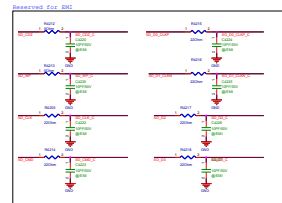
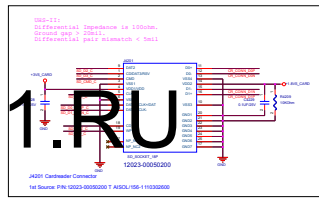
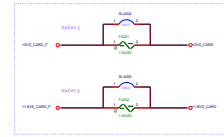
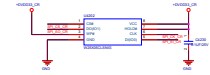
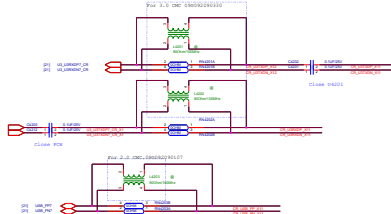
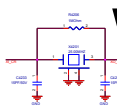
ASUS NGFF M-KEY PCIe4 Connector HW-BOM
1st Source: P/N: 12000-02100000 AR9301/NA9300-96701-1580

Table 8-5. Power Supported Normal and Low-temperature Configurations

Power Mode				Temperature															
Power Mode	Power State	Power State	Temperature	Temperature															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
Normal	D0	D0	Normal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14		
Low-temperature	D0	D0	Normal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14		
Low-temperature	D0	D0	Normal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14		
Low-temperature	D0	D0	Normal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14		
Low-temperature	D0	D0	Normal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

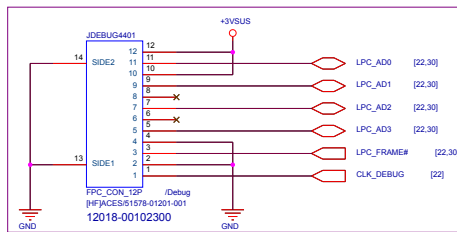
1. The power supported by the device is determined by the device and the highest temperature. When power is supported by the device, the power supported by the device is determined by the device and the highest temperature.

System	ASUS NGFF M-KEY PCIe4 Connector HW-BOM	ASUS NGFF M-KEY PCIe4 Connector HW-BOM
PCIE 000	1	1
PCIE 001	1	1



LPC Debug Port

R2.0-12 R1.1-17



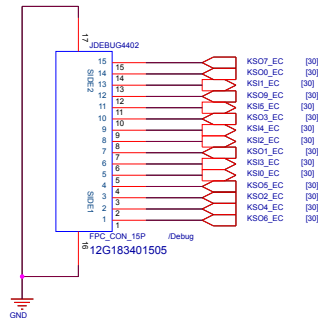
JDEB4401 Connector (MP USE)

1st Source: P/N:12018-00102300 ACES/51578-01201-001

2nd Source: P/N:12018-0102300 ENR/51578-01201-001

R2.0

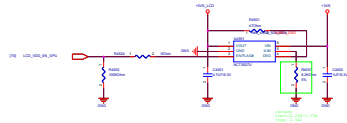
Main Board



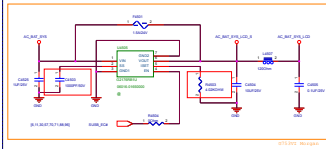
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ASUS		Project Name	Rev
G703GI			R2.1
Title : BUG_LPC			
Size	ASUSTeK COMPUTER INC. Engineer: NB1 RD2 EE1		
A			
Date: Thursday, January 18, 2018	Sheet	44	of 103

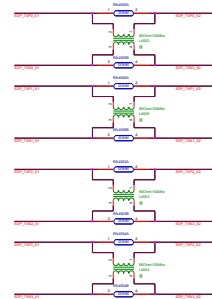
LCD Power switch



Panel BL Power



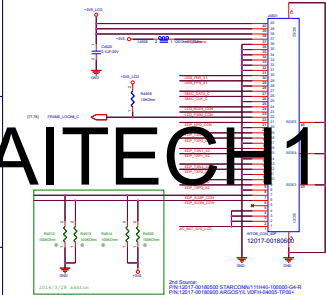
For EMI



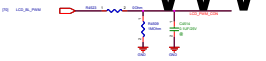
eDP circuit



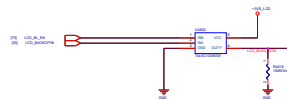
eDP Panel Conn.



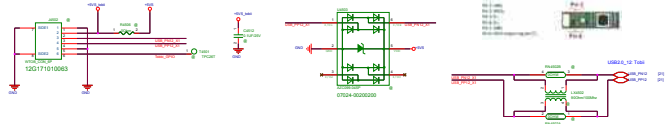
eDP_BL PWM



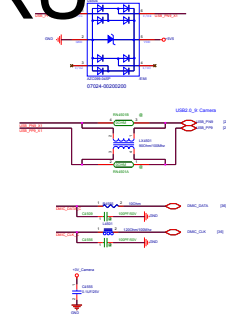
eDP_BL_EN



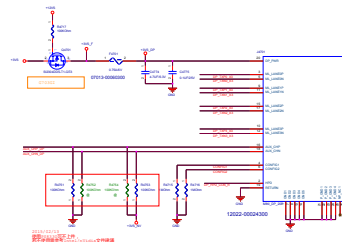
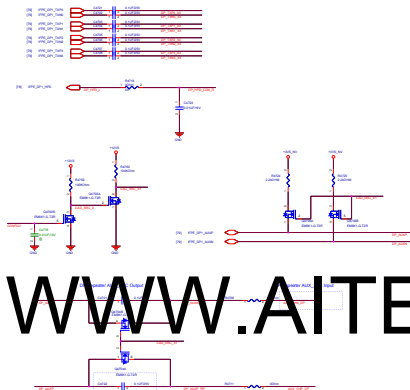
Tobii IS4 Conn.



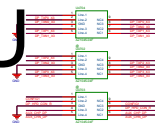
Camera & MIC

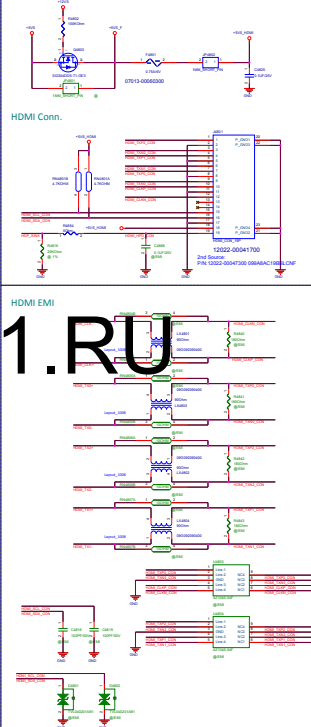


DP Repeater_PS8330B

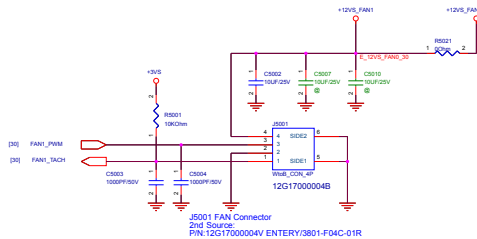


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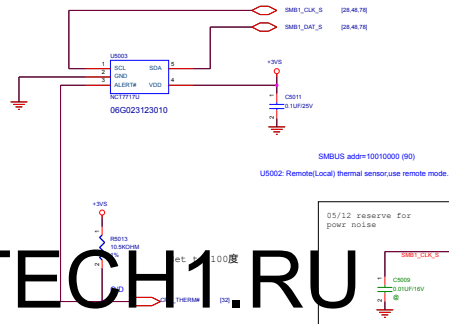




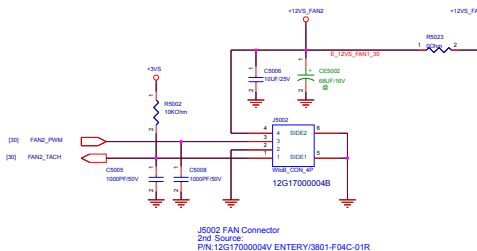
PWM CPU Fan



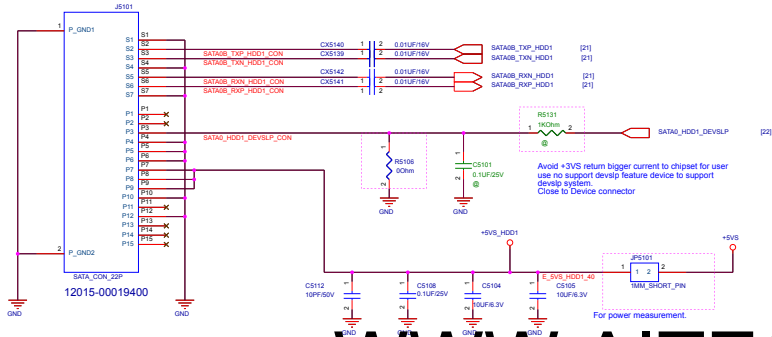
CPU Thermal Sensor



PWM VGA Fan

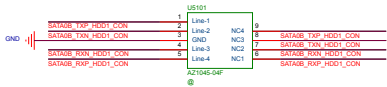


HDD, SATA Port0



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EMI Request



1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

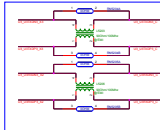
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

[illegible]

Figure 1 shows four DNA constructs (a, b, c, d) used in the study. Each construct is a 1.5 kb DNA fragment containing a 0.5 kb EcoRI-XbaI fragment. The constructs are: (a) pCMV-EGFP, (b) pCMV-EGFP-EGFP, (c) pCMV-EGFP-EGFP-EGFP, and (d) pCMV-EGFP-EGFP-EGFP-EGFP. The constructs are shown as double-stranded DNA with the EcoRI and XbaI sites indicated by vertical lines. The EGFP gene is shown as a blue box. The constructs are labeled with their respective names and the size of the fragments.



USB3.0 EMI-Protection



```

[0000]
00000000, 00000000, 00000000, 00000000
0000 00000000 00000000 00000000 00000000

```

ESD PROTECTION
1st Source: PIN 07024-01380000 ESD PROTECTION A21863-018

Term	Channel Enable [EN]	Receiver Detects [RDET_OK]
0 : 0/2 (n-0/2)	Disable	Disable
1 : 0/2 (n-1/2)	Enable(Default)	Enable(Default)
Note	Channel Enable / Receiver detection with internal 100K pull-up R.	

USB3.1 Port 1

USB3.1 PHY IC (7200)

USB3.1 Port 1 Connector

USB3.1 Port 1 Pinout:

- Pin 1: GND
- Pin 2: D+
- Pin 3: D-
- Pin 4: D+
- Pin 5: D-
- Pin 6: GND
- Pin 7: GND
- Pin 8: GND
- Pin 9: GND
- Pin 10: GND
- Pin 11: GND
- Pin 12: GND
- Pin 13: GND
- Pin 14: GND
- Pin 15: GND
- Pin 16: GND
- Pin 17: GND
- Pin 18: GND
- Pin 19: GND
- Pin 20: GND
- Pin 21: GND
- Pin 22: GND
- Pin 23: GND
- Pin 24: GND
- Pin 25: GND
- Pin 26: GND
- Pin 27: GND
- Pin 28: GND
- Pin 29: GND
- Pin 30: GND
- Pin 31: GND
- Pin 32: GND
- Pin 33: GND
- Pin 34: GND
- Pin 35: GND
- Pin 36: GND
- Pin 37: GND
- Pin 38: GND
- Pin 39: GND
- Pin 40: GND
- Pin 41: GND
- Pin 42: GND
- Pin 43: GND
- Pin 44: GND
- Pin 45: GND
- Pin 46: GND
- Pin 47: GND
- Pin 48: GND
- Pin 49: GND
- Pin 50: GND
- Pin 51: GND
- Pin 52: GND
- Pin 53: GND
- Pin 54: GND
- Pin 55: GND
- Pin 56: GND
- Pin 57: GND
- Pin 58: GND
- Pin 59: GND
- Pin 60: GND
- Pin 61: GND
- Pin 62: GND
- Pin 63: GND
- Pin 64: GND
- Pin 65: GND
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- Pin 81: GND
- Pin 82: GND
- Pin 83: GND
- Pin 84: GND
- Pin 85: GND
- Pin 86: GND
- Pin 87: GND
- Pin 88: GND
- Pin 89: GND
- Pin 90: GND
- Pin 91: GND
- Pin 92: GND
- Pin 93: GND
- Pin 94: GND
- Pin 95: GND
- Pin 96: GND
- Pin 97: GND
- Pin 98: GND
- Pin 99: GND
- Pin 100: GND

The diagram shows a power electronic circuit for a 4-quadrant converter. It consists of a full-bridge inverter (top) and a diode rectifier (bottom). The inverter is formed by four IGBTs (labeled IGBT1, IGBT2, IGBT3, IGBT4) with anti-parallel diodes. The rectifier is formed by four diodes (labeled D1, D2, D3, D4). The DC link is connected to a 100V source. The AC output is connected to a load. The circuit is labeled with 'IGBTs' and 'Diodes'.

1st Source: PIN:27024-0020220 AMAZINGAJZC089-045P .JRTD
2nd Source: PIN:27024-0070000 N3XPLUS8236D

< EQ table for Pericom 1002B >

SSGA-E	Gen 1 (#2 SSNA-pH)	Gen 2 (#2 SSNA-pH)
0-0-D to SNG	5.1	10.8
8-Feed to SNG	1.9	6.7
7-Leave Open	1.2 (2x fault)	8.9 (2x fault)
1-0-D to VOD	6.8	11.1

Note: With interval 120kton pull-up Rap and 200kton pull-down follows.

Red = 68kton

AG33-8	F101 Gain [dB]
0 : EO to GND	-3.0
8 : Ref to GND	-1.5
F : Input Open	0 (Default)
1 : EO to VDD	+3.0

AQ3.4	Fat Gain (kg)
0 : EO to END	-0.0
5 : Rest to END	-1.5
7 : In-use Open	0 (Default)
1 : EO to VDD	+2.0

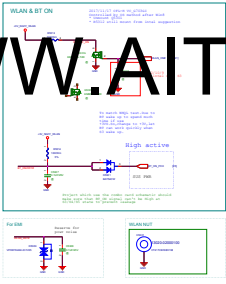
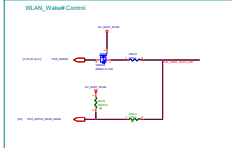
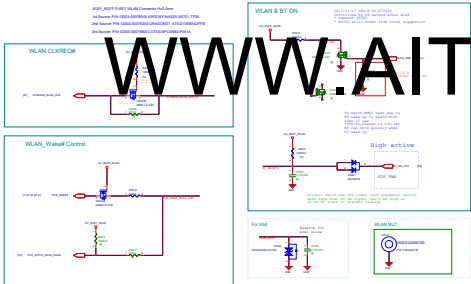
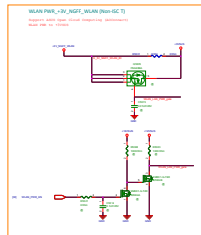
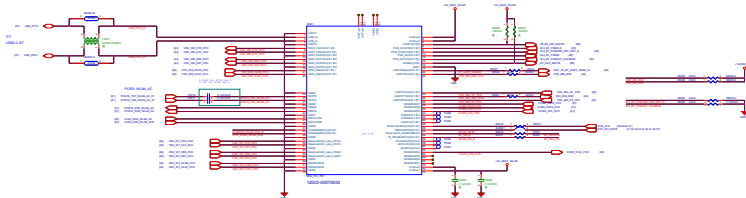
SW[3:0]	Output Linear 1 (mV)
0: EO to GND	800
1: Ref to GND	1200
2: Sensor Open	2000 (Default)
3: EO to VDD	1300

SW[3:0]	Output Linear 1 (mV)
0: EO to GND	800
1: Ref to GND	1200
2: Sensor Open	2000 (Default)
3: EO to VDD	1300

81.1.00

NGFF M.2 TYPE_E-KEY WIFI

Main Board



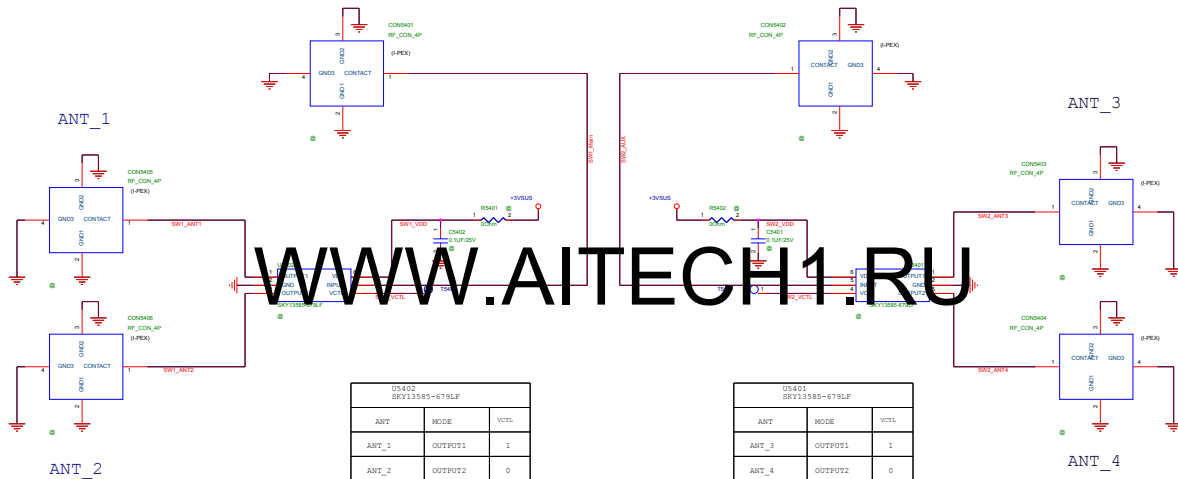
XBOX WLAN Conn.



Pin Header - 20P1	
Pin	Signal
1	VCC
2	GND
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	NC
12	NC
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14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC

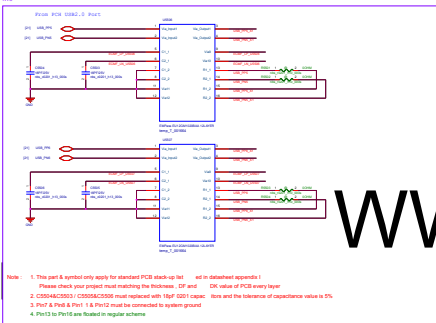
Module_Main

Module_AUX

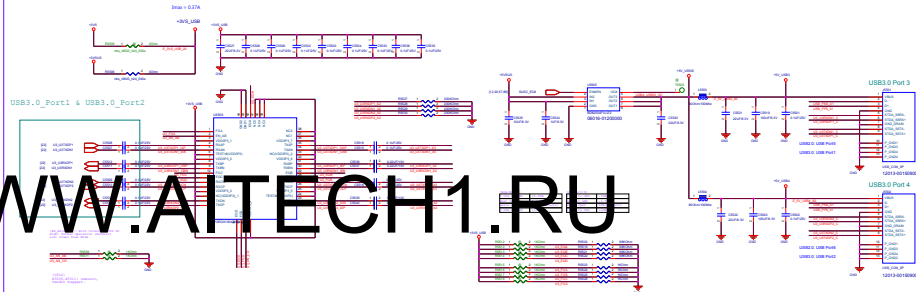


USB2.0 EMI-Protection With ECMF(PCB 1.25mm_12Layer)

Rev



USB3.1 Gen2/Gen1 Redriver :
06113-00270000 PERICOM PI3EQX1004ZHEX

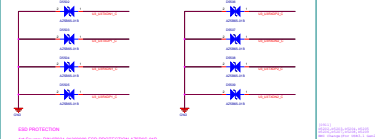


WWW.AITECH1.RU

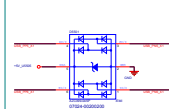
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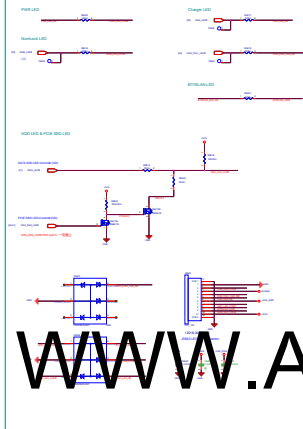
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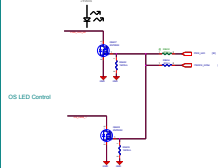
USB2.0 ESD-Protection



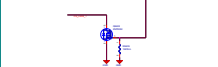
To LED control IO SD Page 40



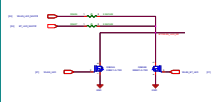
PWR LED Control



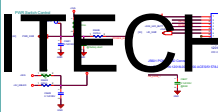
OS LED Control



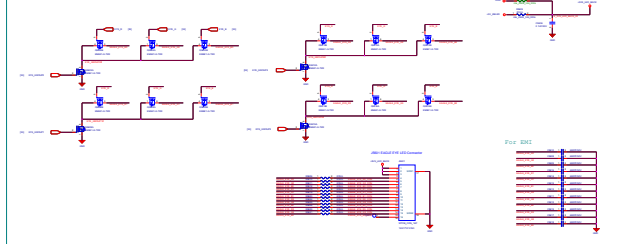
BT/WLAN LED Control



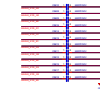
To Power Button IO SD Page 63



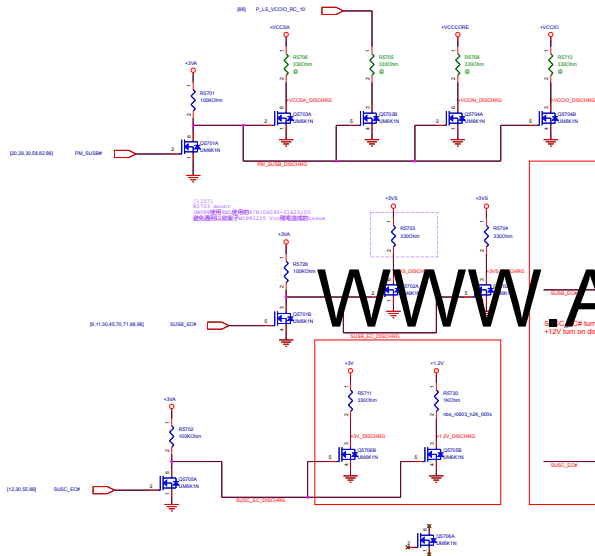
For Eagle Eye LED CTRL



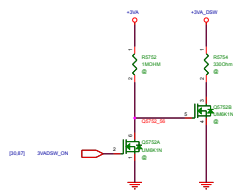
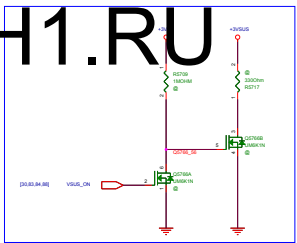
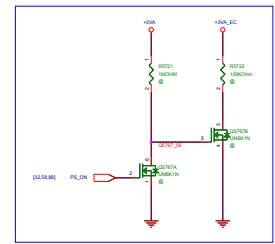
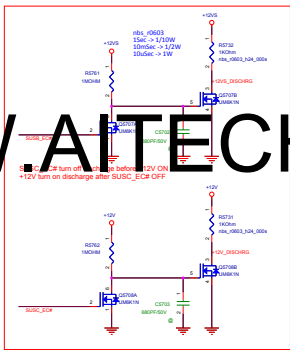
For SPI

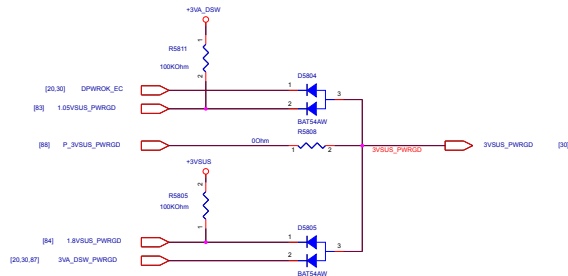


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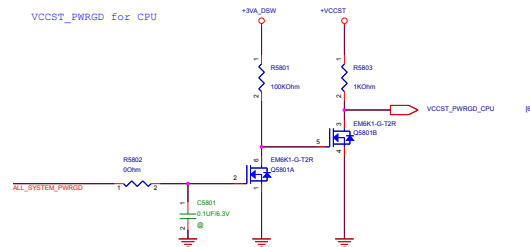


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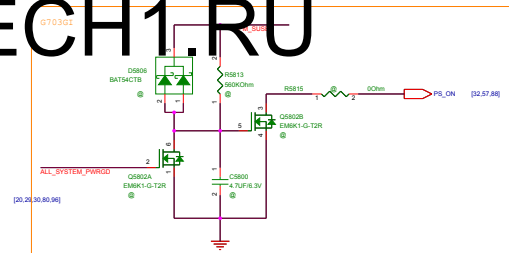
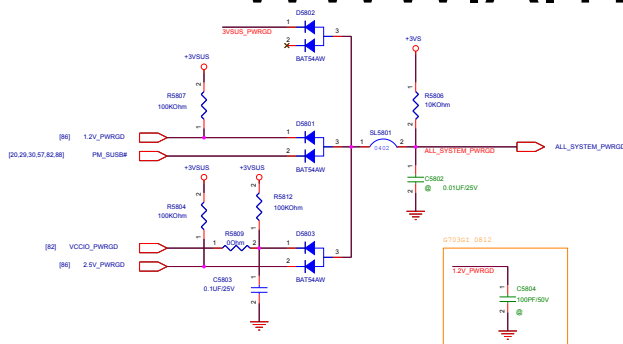


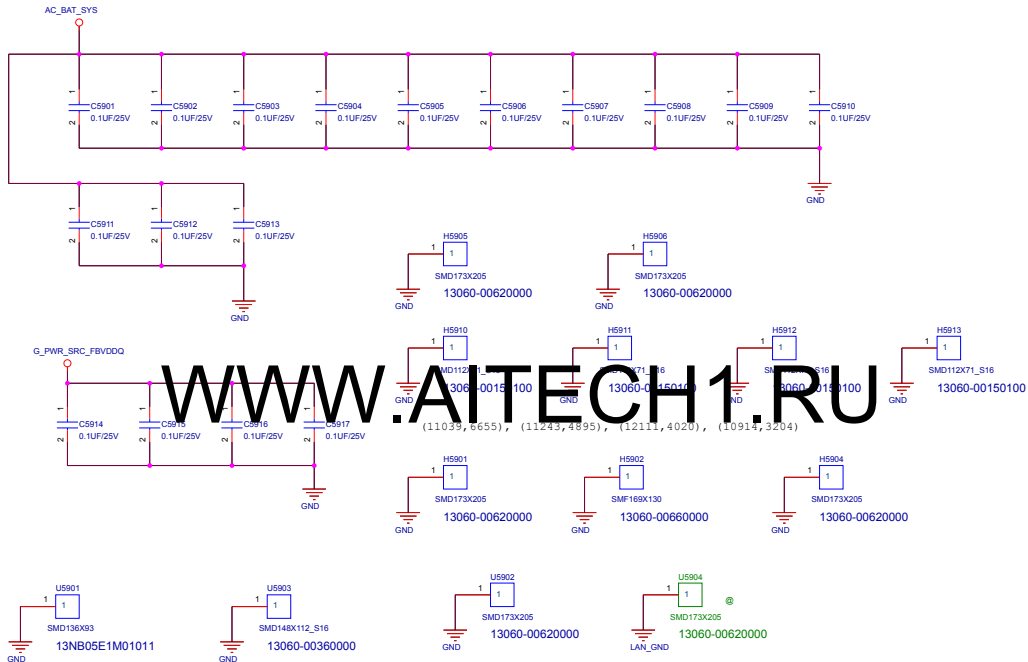


VCCST_PWRGD for CPU




WWW.AITECH1.RU



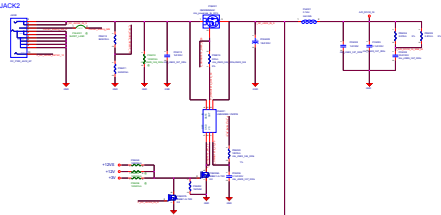


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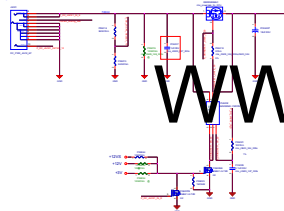
		Project Name	Rev
G703GI			R2.1
Title : EMI			
Size	Dept.: ASUSTeK COMPUTER INC. Engineer:		
A			
Date: Thursday, January 18, 2018	Sheet		59 of 103

DC-IN Connector

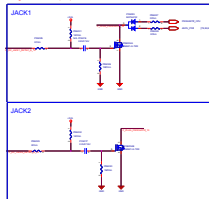
JACK2



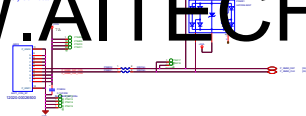
JACK1



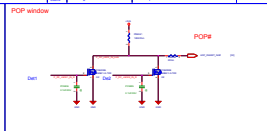
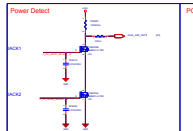
Plug HW Throttle(in)



Battery Connector

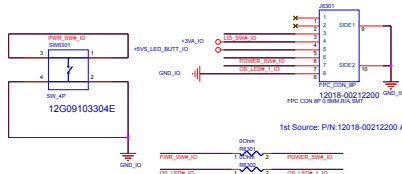
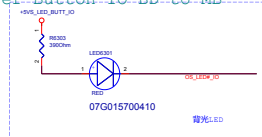


DC-IN Connector	DC-IN Connector	DC-IN Connector
Pin 1	Pin 1	Pin 1
Pin 2	Pin 2	Pin 2
Pin 3	Pin 3	Pin 3
Pin 4	Pin 4	Pin 4



WWW.AITECH1.RU

Power Button IO BD to MB

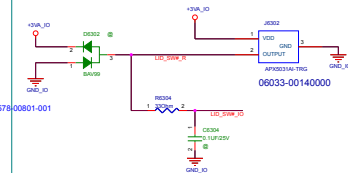


1st Source: PIN-12018-00212200 ACES/51578/00901-001

2nd Source: PIN-12009-00040500 DAWNING/TS-A52-2-S017

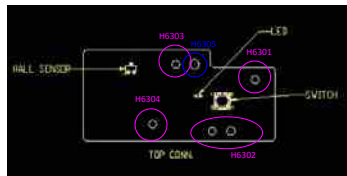
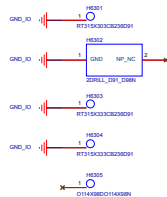
(10914)
C6301, C6302, C6303, C6305: ROHM
SMT

LID Switch

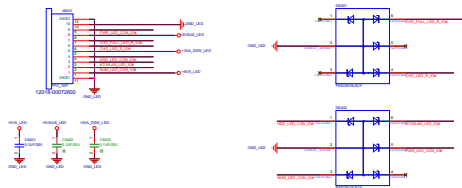


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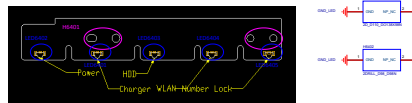
Nut & Screw Hole



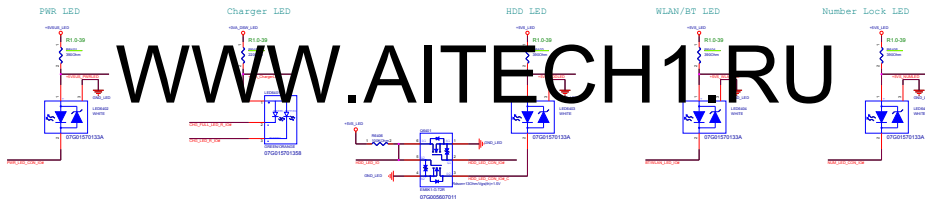
LED IO BD to MB



Nut & Screw Hole

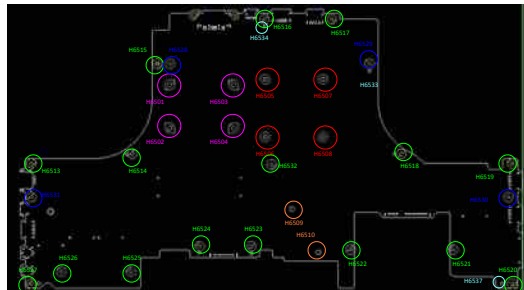
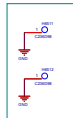


Functions LED



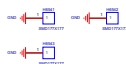
WWW.AITECH1.RU

TOP SKEW HOLE & PAD

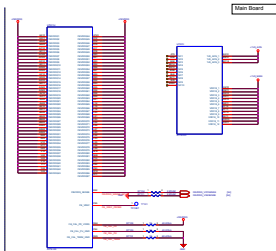
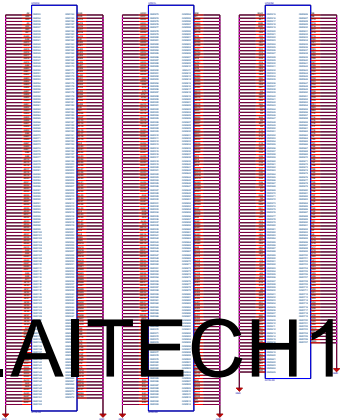
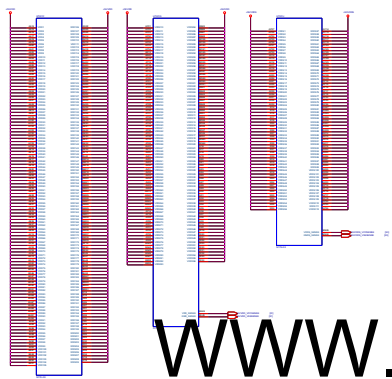


CPU bracket

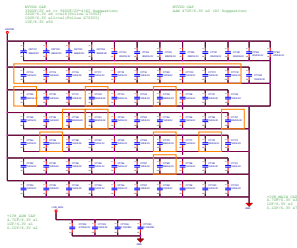
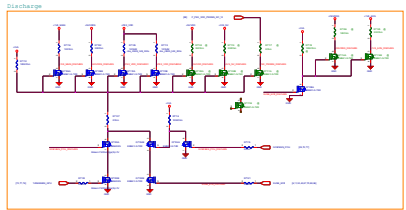
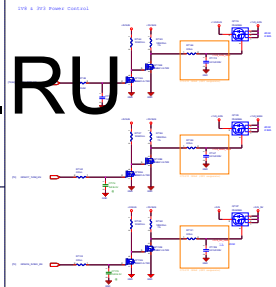
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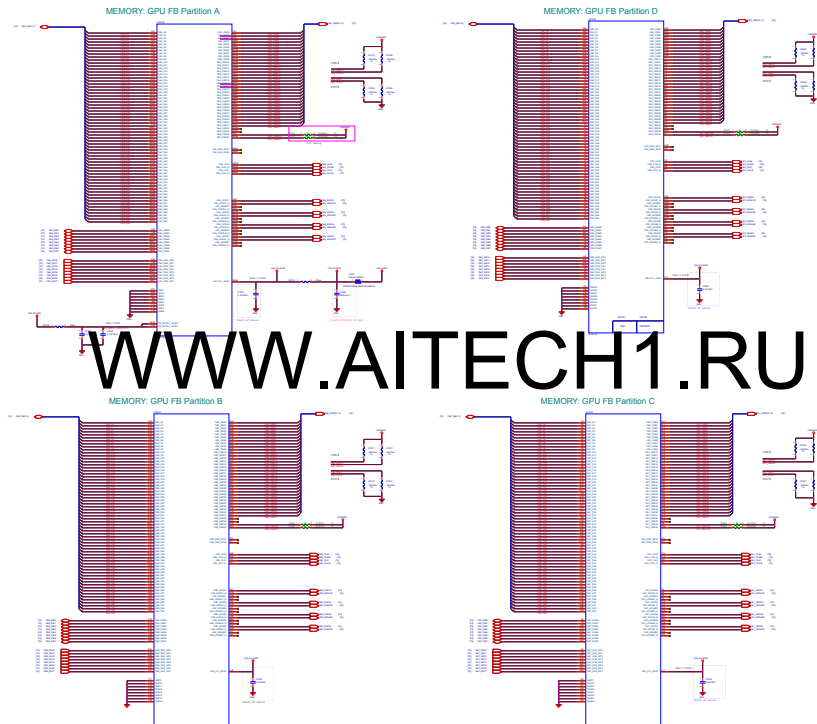


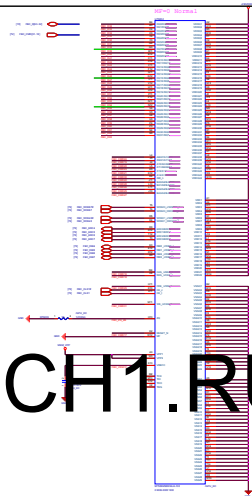
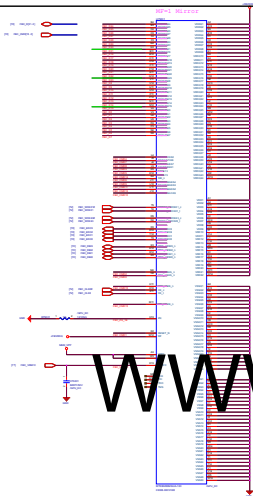
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WWW.AITECH1.RU

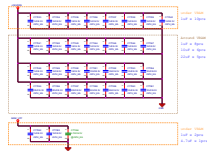
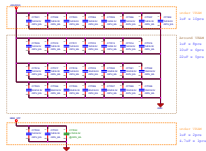




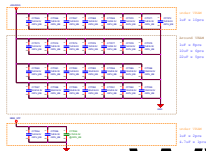


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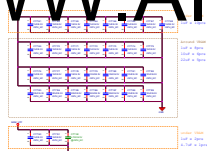
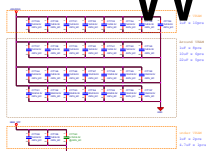
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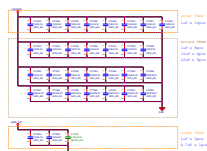
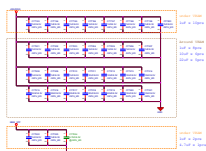
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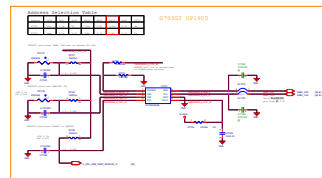
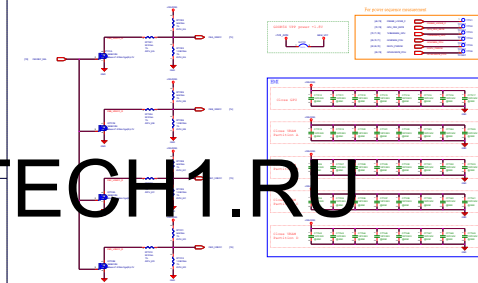
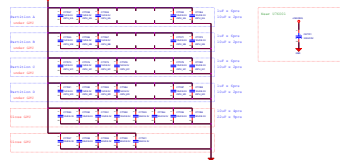
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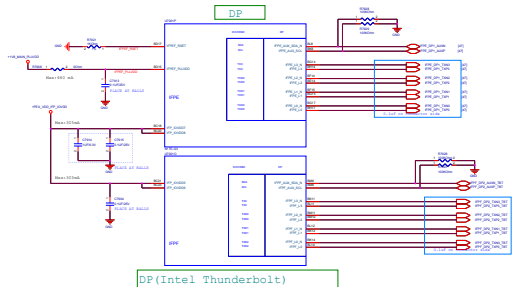
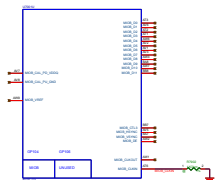
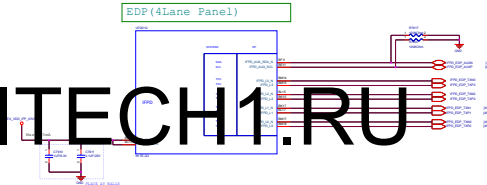
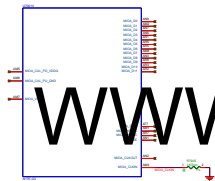
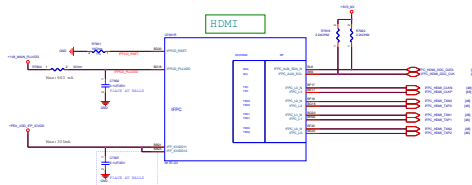
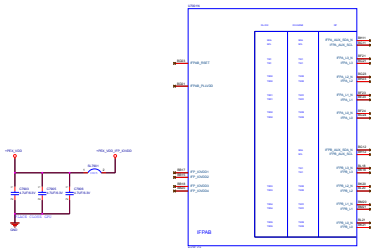


Channel D



VMAIN_PWR_F0000



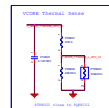
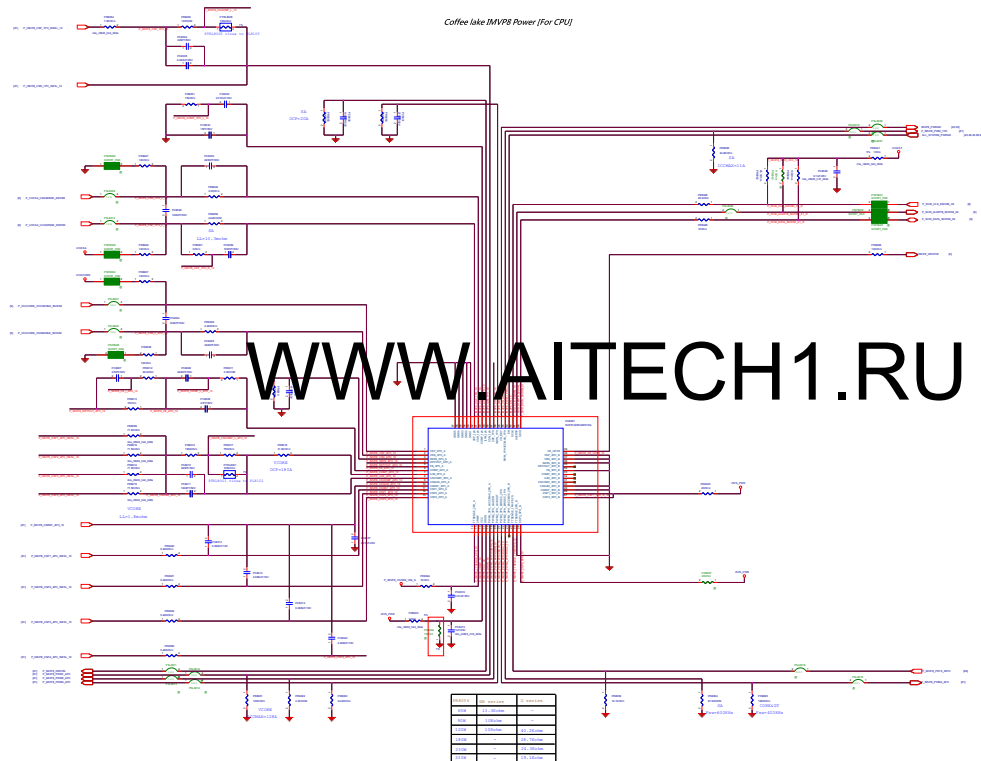


15.1.3 Unreacted ligands mC_2H_5

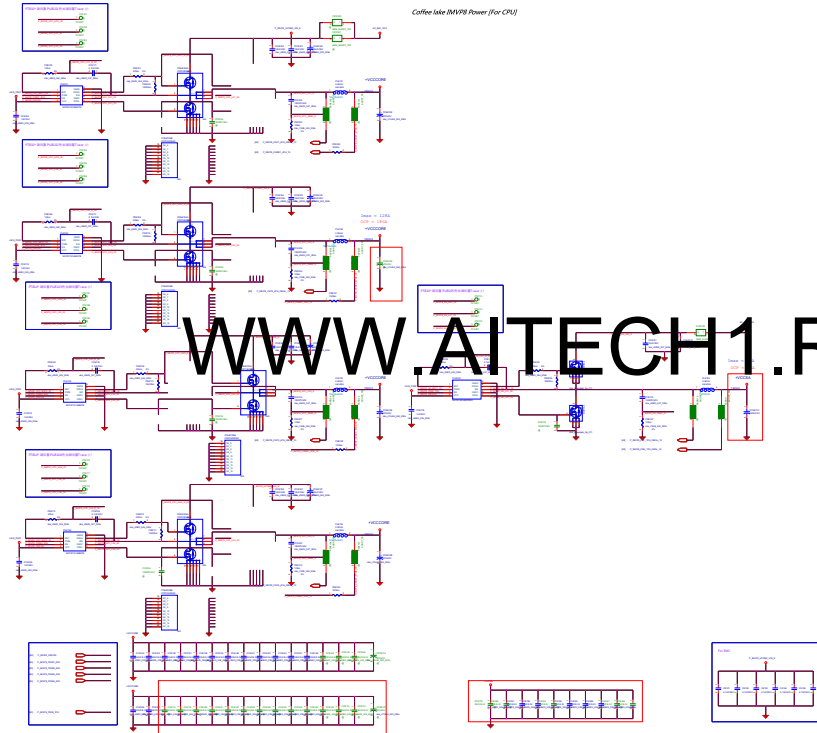
The following provided authors agreed with the review:

• *Proceedings of 55th AGU*

Coffee lake IMVP8 Power (For CPU)

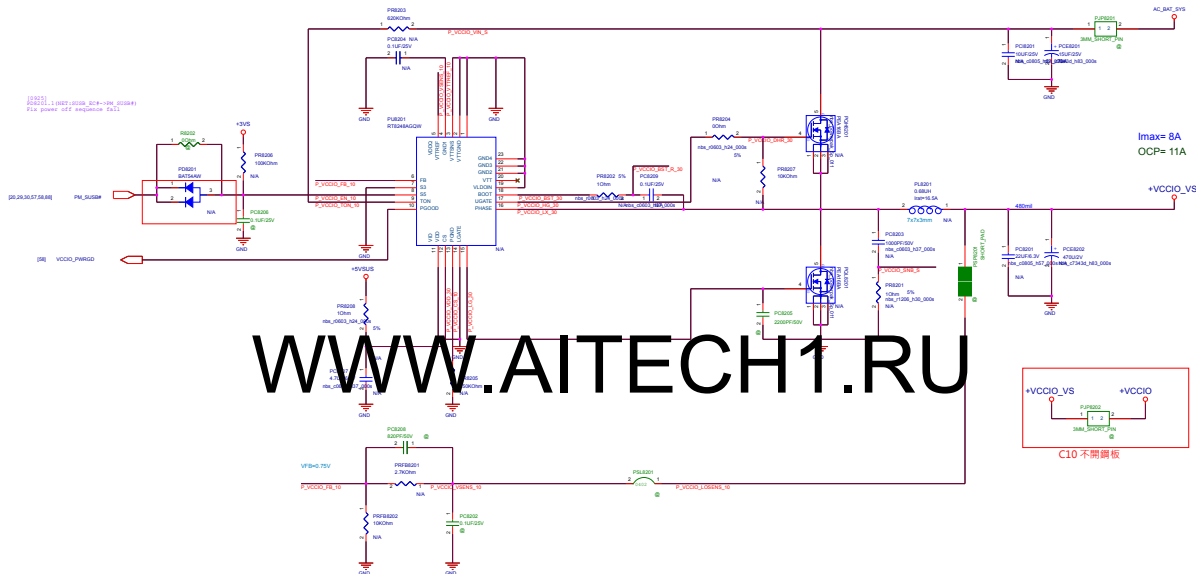


Coffee lake (MVP) Power (For CPU)

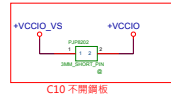


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+VCCIO [For CPU]



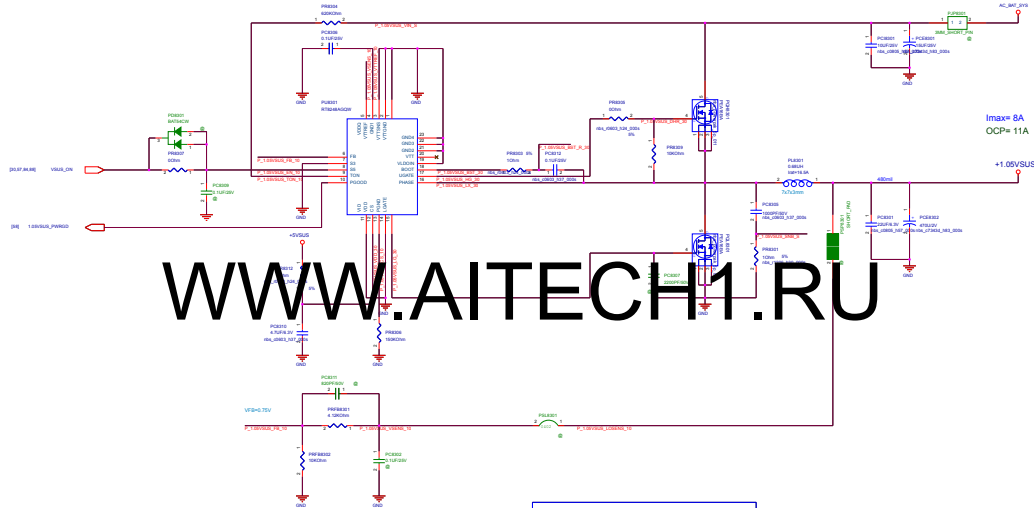
WWW.AITECH1.RU



PT820* 請放置 PU8201旁;並請放置Trace 上

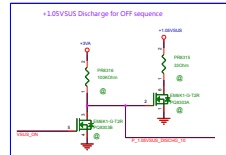


+1.05VSUS [For PCH]

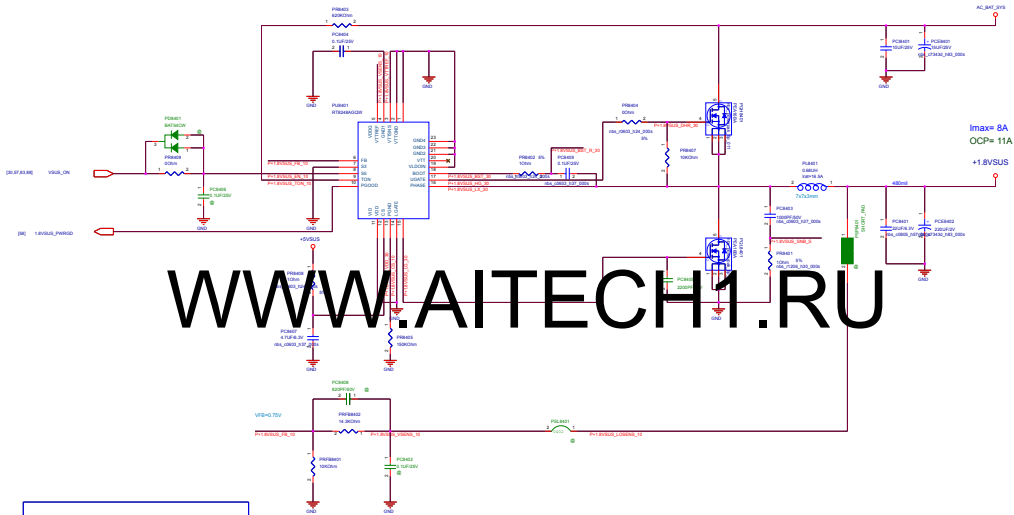


Imax= 8A
OCP= 11A

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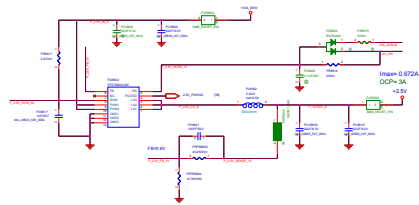
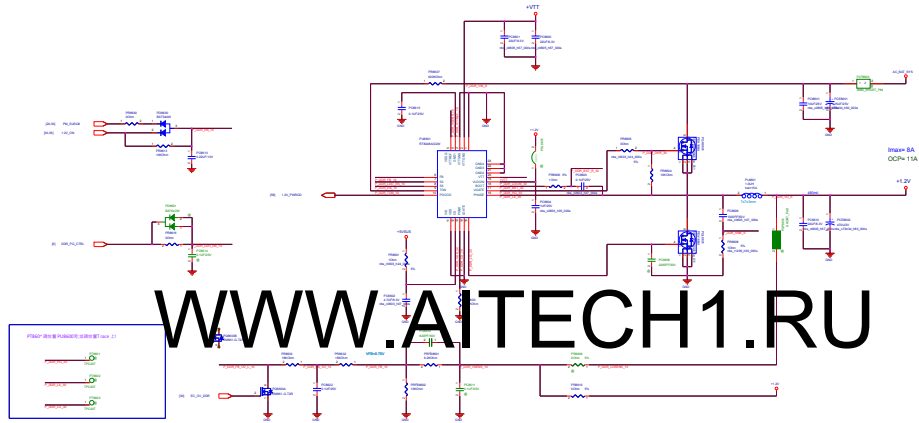
+1.8VSUS [For PCH]



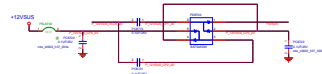
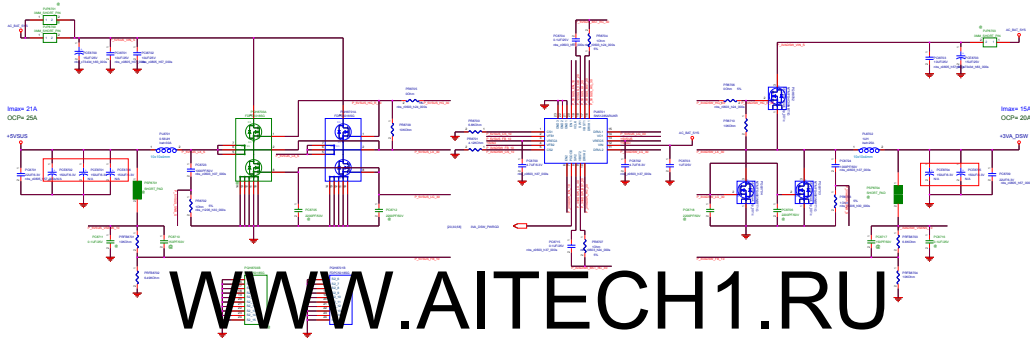
PT840* 請放置 PU8401旁;並請放置Trace上!



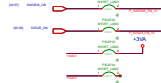
+1.2V / +VTT / +2.5V[For Memory]



+3VA_DSU / +5VSUS [System Power]



※ Check 電源規格 +12VSUS 10A 電源規格電圧不適合時 10A/10V

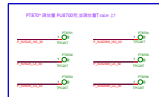


Adaptor Mode (200W)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
PS+5V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

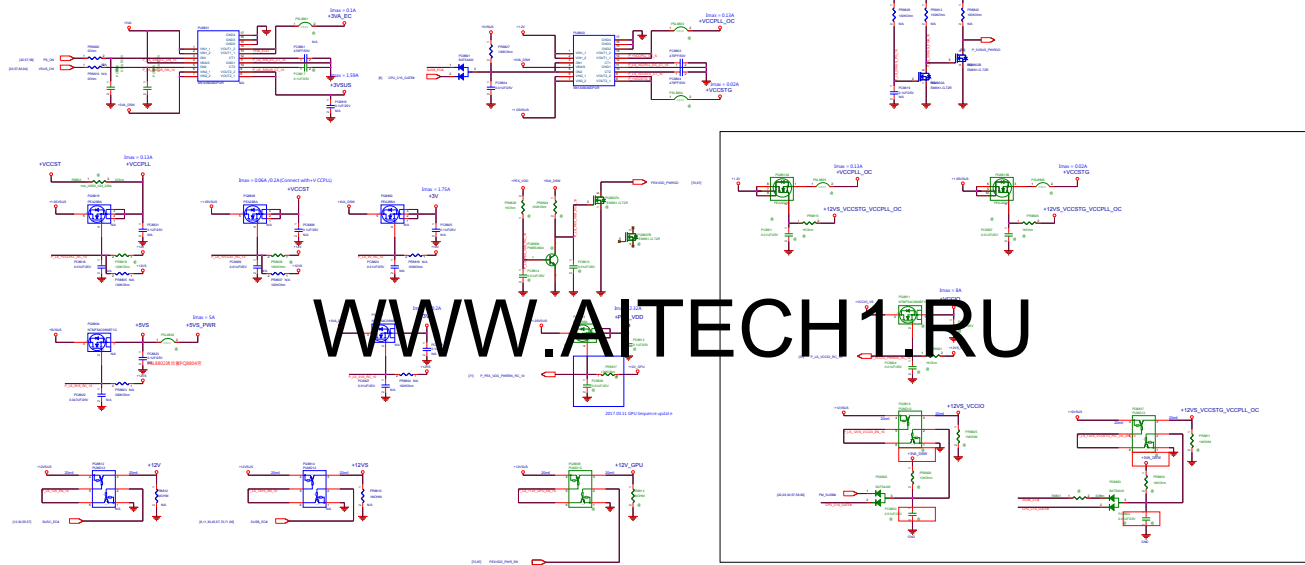
Battery Mode (200W)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
PS+5V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100



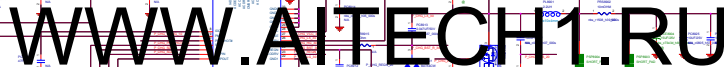
Load Switch

Main Board



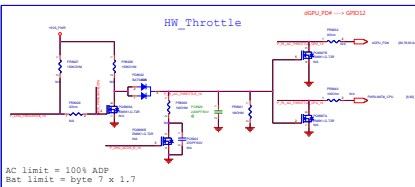
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华硕C10G703GI 使用CPU PEG， 测试华硕C10， 详细



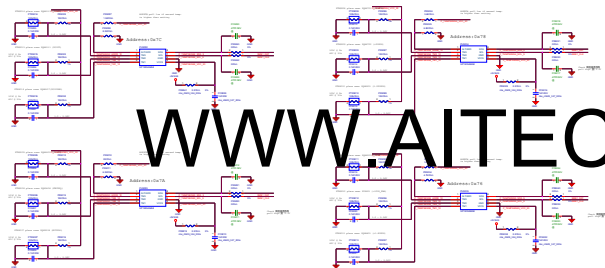
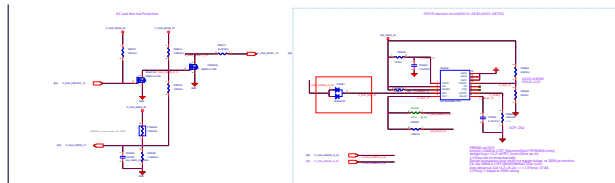
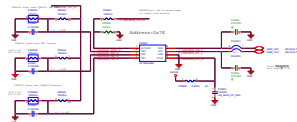
Adaptor select
total power = 90% ADP

Adaptor select			
		B Series	C Series
PRE921		10m	5m
PRE936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
500K	2.8V	120W	400W



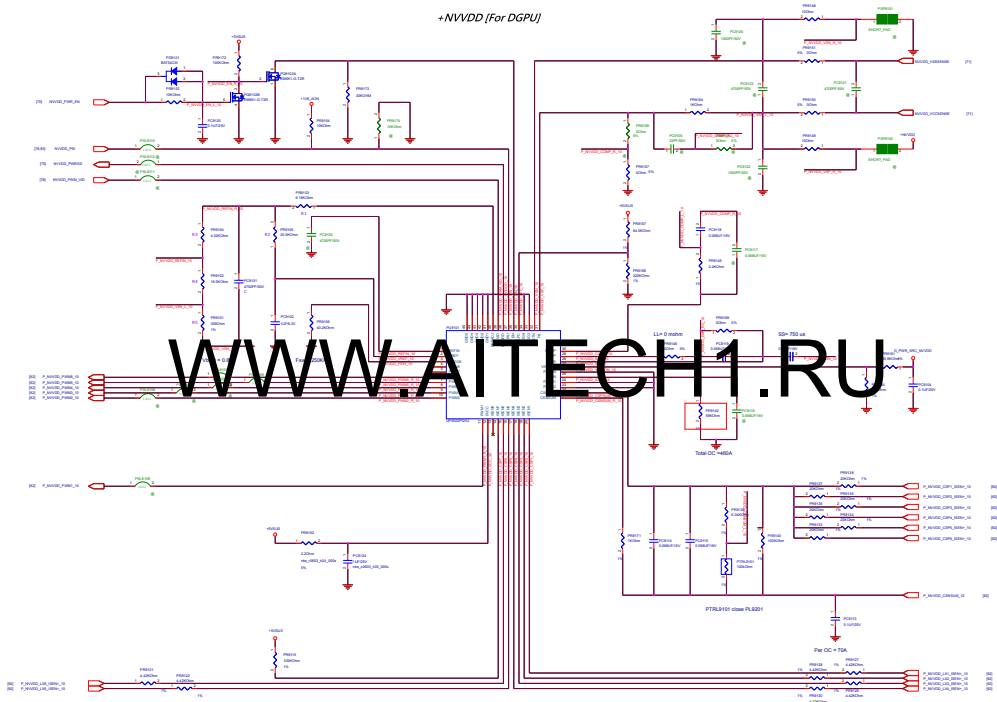
Address	Value
0x00	0x00
0x01	0x00
0x02	0x00
0x03	0x00
0x04	0x00
0x05	0x00
0x06	0x00
0x07	0x00
0x08	0x00
0x09	0x00
0x0A	0x00
0x0B	0x00
0x0C	0x00
0x0D	0x00
0x0E	0x00
0x0F	0x00

Register Address	Value
0x00	0x00
0x01	0x00
0x02	0x00
0x03	0x00
0x04	0x00
0x05	0x00
0x06	0x00
0x07	0x00
0x08	0x00
0x09	0x00
0x0A	0x00
0x0B	0x00
0x0C	0x00
0x0D	0x00
0x0E	0x00
0x0F	0x00

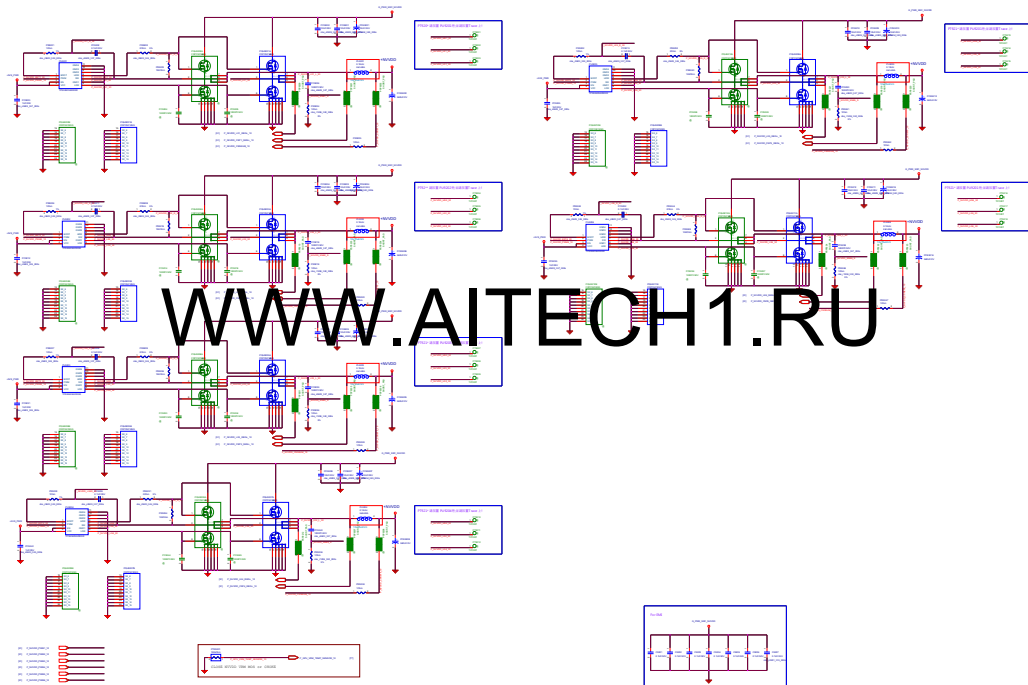


WWW.AITECH1.RU

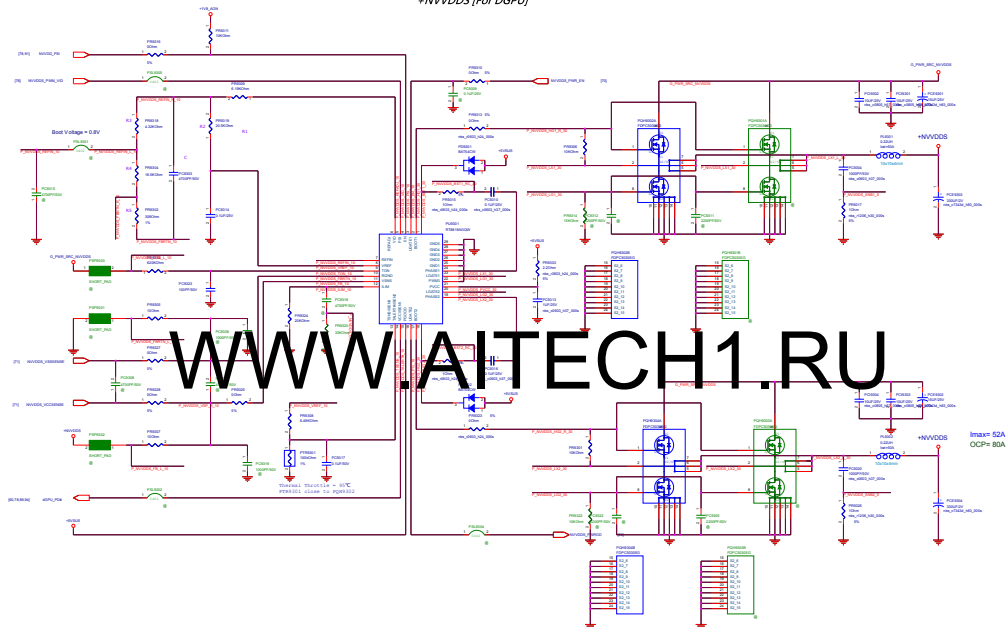
+NVVDD [For DGPU]



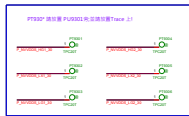
+NVVDD (For DGPU)



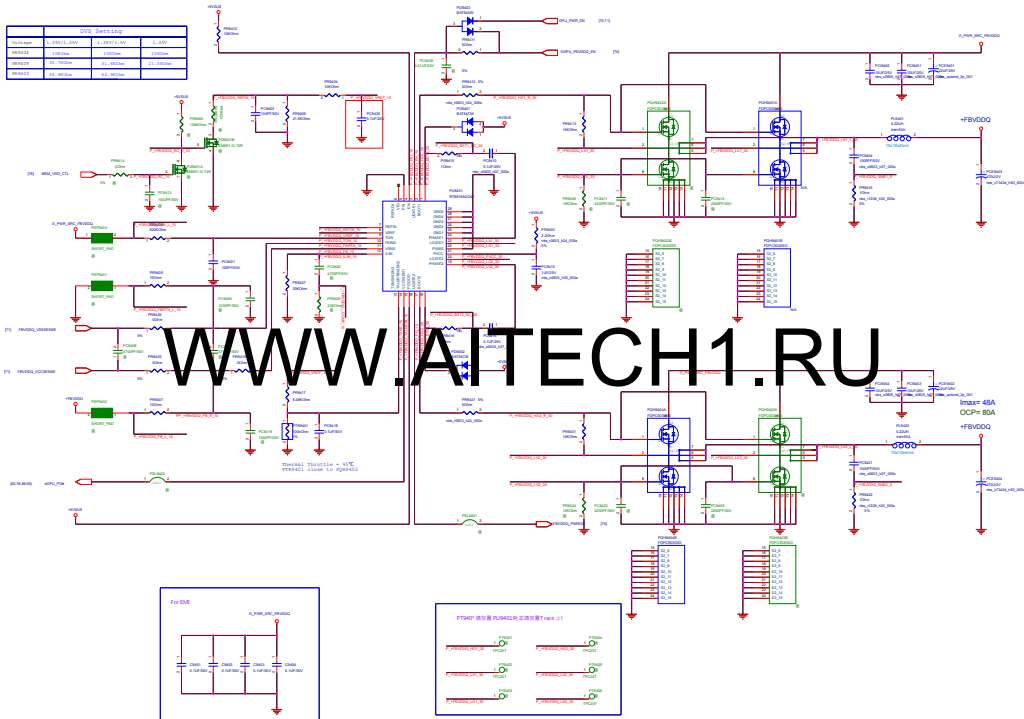
+NVVDDS (For DGPU)



Imax= 52A
OCP= 80A

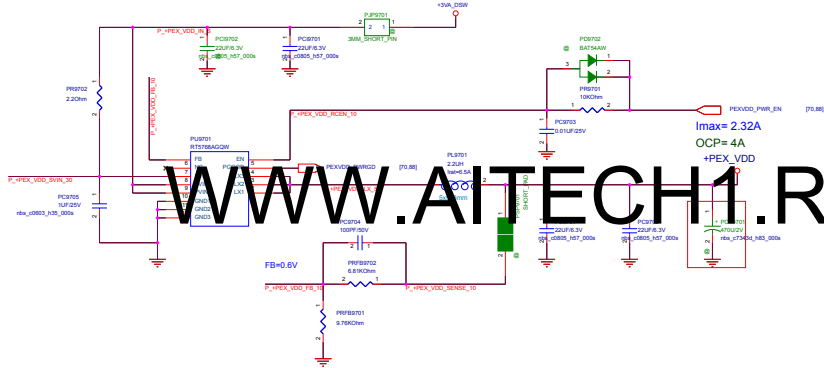


+FBVDDQ [For VRAM]





PEX_VDD [For GPU]

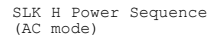


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```

C:CPU                                     (+RTCSTAT)+3VA_RTC
P:PCR                                   (AC_BAT_STS)+3VA/+5VA
S:PLT                                  (+3VA_RTC)RTCSTA(PCH)
Power                                (Power)(AC_IM_OC(PCH)
Signal                               (EC)PS_ON(+3VA_EC)
                                      (PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSM(+3VA_DSM_PWRGD)
(ECDPNWRC)(EC_PCH)
(+3VA_DSM_PWM_BATLOW#(PCH)
(PCH)PM_SLP_SUSB#(EC)
(VBUS_ON)+1.0V_USB_VCCPIN(1.0VBUS_PWRGD)
(EC)PM_RMRST#_PCH(PCH)
(PCH)SUBWARN#(EC)
(EC)HE_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR_Switch)PWR_SW#(EC)
(EC)PM_FWBSTH#(PCH)
(EC)SUBC_EC#(Power)
(SUBC_EC#)+12V/+5V/+3V
(EC)SUBS_EC#(Power)
(SUBS_EC#)+12VS/+5VS/+3VS
(VBUS_ON)+1.0V_VCCST,VCCPLL(VCCST_PWRGD)
(=VCCIO)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(=12VS)+VCCPLL_OC
(SUBS_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(INV9,PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(PWRGD)
(Power)1.2V_PWRGD(AND)
(Power)INV9_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD,CPU(CPU)
(EC)PM_PNRKC_PCH(PCH)
(PCH)CLK_PCH_BCLR(PCH)
(PCH)R_CHIPUPMGD(CPU)
(ALL_SYSTEM_PWRGD)P_INV9_EN_10(Power)
(CPU)P_SVID_XATA_12(Power)
(EC)PM_SYSNWRK_PCH(PCH)
(PCB)PLT_RST#(CPU/EC/Device)
(P_INV9_DRVIN)+VCCORCE(INV9_PWRGD)
(CPU)H_THERMTRIP4(PCH)
(PCH)DDR4_DRAMST#(Memory)
+VDD

```



SLK H Power Sequence
(DC mode)